

SuperQ® 250V N-Channel Power MOSFET

35mΩ, 39A, PDFN 5X6

FEATURES

- Industry-leading resistance in PDFN 5X6 package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production, 175°C rated
- Low switching losses, Q_{SW} and E_{OSS}
- Easier paralleling with $\pm 0.5V$ gate threshold

APPLICATIONS

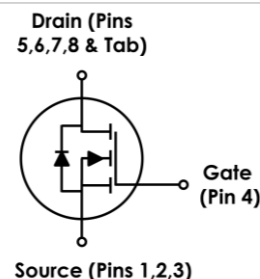
- Isolated DC/DC modules
- LED Lighting
- Boost converters and SMPS control FETs
- Motor Drive

PRODUCT SUMMARY

Parameter	Typ	Max	Unit
V_{DS}		250	V
$R_{DS(on)}$ @ 10V	30	35	mΩ
I_D		39	A
Q_G	28	36	nC
Q_{SW}	2.7		nC
E_{OSS}	1.4		μJ

DESCRIPTION

Engineered for isolated DC/DC modules and high-efficiency SMPS and motor drives, this 250V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust PDFN 5X6 package. Featuring low $R_{DS(on)}$ and Q_{SW} , it minimizes heat dissipation at both full and partial loads.



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS25M035S1C	PDFN 5X6	iS25M035S1	13" 5,000pcs T&R

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), $TC = 25^\circ\text{C}$	39	A
	Continuous drain current (silicon limited), $TC = 100^\circ\text{C}$	28	
I_{DM}	Pulsed drain current	143	
I_S	Continuous diode forward current, $TC = 25^\circ\text{C}$	39	
$I_{S,PULSE}$	Diode pulse current	143	
P_D	Power dissipation, $TC = 25^\circ\text{C}$	125	W
T_J, T_{SG}	Operating junction, storage temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse $I_D = 8.9A$, $R_{GS} = 25\Omega$	39	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance – PDFN 5X6	-	-	1.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	$^\circ\text{C}/\text{W}$

(1) 40mm x 40mm x 1.5mm epoxy PCB FR4 with 6cm² (one-layer, 70μm thick) copper area for drain connection. PCB is vertical in still air.

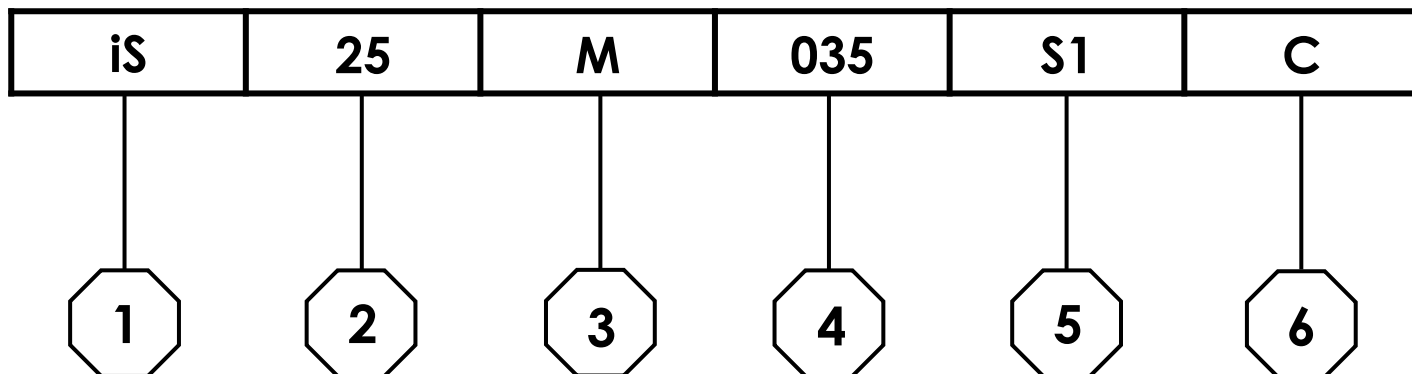
ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	250	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 200V, T _J = 25°C	-	-	1.0	μA
		V _{GS} = 0V, V _{DS} = 200V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	-	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 70μA	3.1	3.6	4.1	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 10A	-	30	35	mΩ
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 125V, f.= 100kHz	-	1,865	2,425	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	12	16	
C _{oss}	Output capacitance ⁽²⁾		-	94	122	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 125V, V _{GS} = 0V	-	284	-	
R _g	Series gate resistance	f = 1MHz	-	4.5	6.8	Ω
T _{d(on)}	Turn-on delay time	V _{DS} = 125V, V _{GS} = 10V, I _{DS} = 10A, R _{G,EXT} = 0Ω	-	TBD	-	ns
T _r	Rise time		-	TBD	-	
T _{d(off)}	Turn-off delay time		-	TBD	-	
T _f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q _g	Gate charge total ⁽²⁾	V _{DS} = 125V, I _D = 10A, V _{GS} = 0 to 10V	-	28	36	nC
Q _{sw}	Switching charge ⁽³⁾		-	2.7	-	
Q _{gd}	Gate to drain charge ⁽²⁾⁽³⁾		-	1.2	1.6	
Q _{g(th)}	Gate charge at threshold ⁽³⁾		-	6.6	-	
Q _{gs2}	Gate to source charge ⁽³⁾		-	1.3	-	
V _{plateau}	Gate plateau voltage		-	5.7	-	V
Q _{oss}	Output charge ⁽²⁾	V _{DS} = 0 to 125V, V _{GS} = 0V	-	137	178	nC
E _{oss}	Capacitive stored energy		-	1.4	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 10A, V _{GS} = 0V	-	1.0	1.2	V
Q _{RR}	Reverse recovery charge	V _{DS} = 125V, I _F = 10A,	-	550	-	nC
t _{rr}	Reverse recovery time	di/dt = 100A/μs	-	105	-	ns

(2) Defined by design. Not subject to production test

(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for definitions of gate charge. For more information, see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING

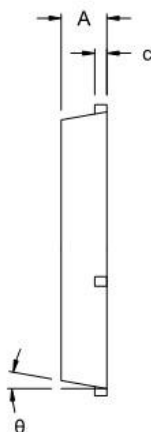
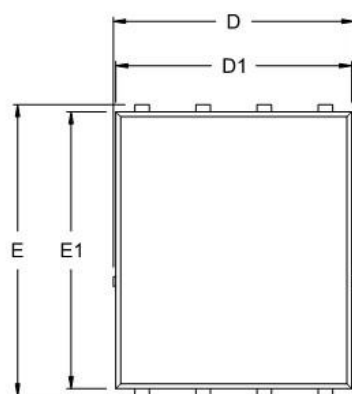
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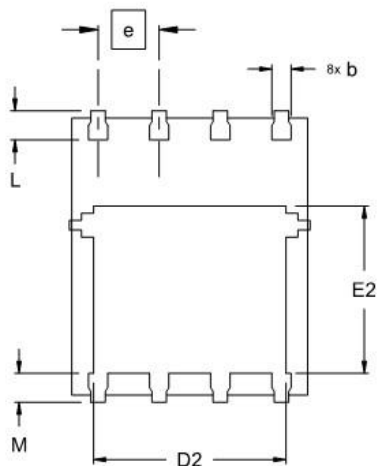
	— iDEAL Semiconductor product
	— Voltage rating divided by 10 (250V)
	— M = N-Channel MOSFET, Standard Threshold
	— Maximum drain-to-source resistance
	— SuperQ® Generation
	— C = PDFN 5X6mm

Package Drawing

PDFN 5X6mm Package



SYMBOL	MIN	MAX
A	0.95	1.05
b	0.31	0.51
c	0.25 REF	
D	4.94	5.30
D1	4.80	5.1
D2	3.70	4.10
E	5.97	6.35
E1	5.67	6.10
E2	3.37	3.76
e	1.27 TYP	
L	0.51	0.71
M	0.51	0.73
θ	0°	10°



Revision History

Revision History		
Version	Date	Comments
Preliminary 1.0	September 2026	Initial Preliminary Rev 1.0

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design resources:



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