

SuperQ™ 200V N-Channel Power MOSFET

FEATURES

- Low $R_{DS(on)}$ in D2PAK-7L package rated to 175°C
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{sw} and E_{oss}
- Easier parallelling with $\pm 0.5V$ gate threshold

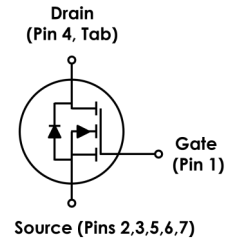
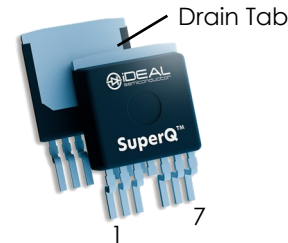
APPLICATIONS

- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

DESCRIPTION

Engineered for high-efficiency motor drives and SMPS, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust D2PAK-7L package. Featuring best-in-class $R_{DS(on)}$ and Q_{sw} , it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY



D2PAK-7L

Parameter	Value	Unit
$T_A = 25^\circ\text{C}$		
V_{DS}	200	V
$R_{DS(on),max}$	7.5	m Ω
I_D	118	A
Q_G	74	nC
Q_{sw}	4.9	nC
E_{oss}	3	μJ



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS20M8R0S1H	D2PAK-7L	iS20M8R0S1	2,000pc Reel

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	118	A
	Continuous drain current (silicon limited), $T_C = 100^\circ\text{C}$	84	
I_{DM}	Pulsed drain current	473	A
P_D	Power dissipation, $T_C = 25^\circ\text{C}$	250	W
T_J, T_{stg}	Operating junction, storage temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse $I_D = 59\text{A}$, $R_{GS} = 25\Omega$	176	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance - D2PAK-7L	-	-	0.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	$^\circ\text{C}/\text{W}$

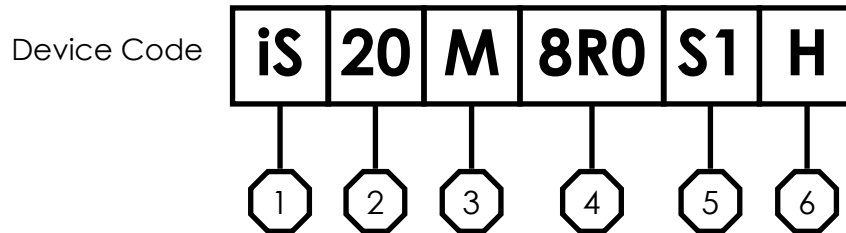
(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.







ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	200	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 160V, T _J = 25°C	-	0.1	1	μA
		V _{GS} = 0V, V _{DS} = 160V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	20	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 213μA	3.1	3.6	4.1	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 26A	-	6.6	7.5	mΩ
g _{fs}	Transconductance	V _{DS} = 10V, I _D = 26A	49	97	-	S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 100V, f = 100kHz	-	5,423	7,159	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	33	44	
C _{oss}	Output capacitance ⁽²⁾		-	206	268	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 100V, V _{GS} = 0V	-	598	-	
R _G	Series gate resistance	f = 1MHz	-	0.9	1.4	Ω
t _{d(on)}	Turn-on delay time	V _{DS} = 100V, V _{GS} = 10V, I _{DS} = 26A, R _{G,EXT} = 0 Ω	-	TBD	-	ns
t _r	Rise time		-	TBD	-	
t _{d(off)}	Turn-off delay time		-	TBD	-	
t _f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q _G	Gate charge total ⁽²⁾	V _{DS} = 100V, I _D = 26A, V _{GS} = 0 to 10V	-	74	96	nC
Q _{sw}	Switching charge ⁽³⁾		-	4.9	-	
Q _{gd}	Gate to drain charge ^{(2) (3)}		-	1.9	2.5	
Q _{G(th)}	Gate charge at threshold ⁽³⁾		-	17.3	-	
Q _{Gs2}	Gate to source charge ⁽³⁾		-	2.9	-	
V _{plateau}	Gate plateau voltage		-	5.5	-	V
Q _{oss}	Output charge ⁽²⁾	V _{DS} = 0 to 100V, V _{GS} = 0V	-	254	327	nC
E _{oss}	Capacitive stored energy		-	3.0	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 26A, V _{GS} = 0V	-	1.1	1.3	V
Q _{rr}	Reverse recovery charge	V _{DS} = 100V, I _F = 26A,	-	709	-	nC
t _{rr}	Reverse recovery time	di/dt = 100A/μs	-	147	-	ns

(2) Defined by design. Not subject to production test.

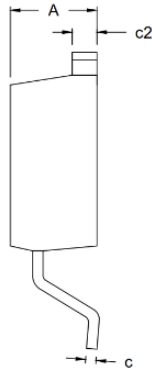
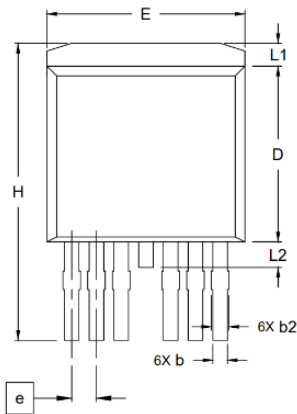
(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING



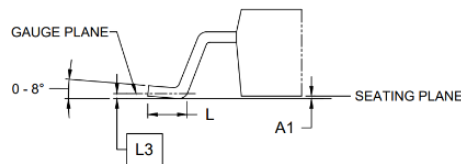
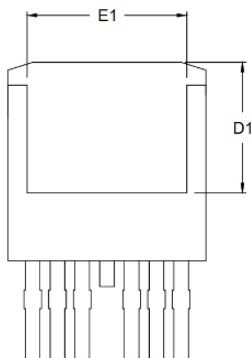
-  — iDEAL Semiconductor product
-  — Voltage rating divided by 10 (200V)
-  — M = N-Channel MOSFET, Standard Threshold
-  — Maximum drain-to-source resistance
-  — SuperQ™ Generation
-  — H = D2PAK-7L

D2PAK-7L Package Drawing



SYMBOL	MIN	MAX
A	4.30	4.70
A1	--	0.25
b	0.50	0.85
b2	0.80	1.00
c	0.40	0.65
c2	1.20	1.40
D	8.50	9.40
D1	6.86	--
E	9.65	10.10
E1	6.50	--
e	1.27 BSC	
H	14.61	15.88
L	1.78	2.79
L1	--	1.60
L2	--	1.78
L3	0.25 BSC	

- Notes:
1. All linear dimensions in millimeters
 2. Dimensions D and E do not include mold flash or protrusions



IMPORTANT NOTICE AND DISCLAIMER

IDEAL SEMICONDUCTOR DEVICES, INC. ("IDEAL") PROVIDES THE DATASHEET AND ALL SUPPORTING DESIGN RESOURCES, SAFETY INFORMATION, AND OTHER MATERIALS (THE "RESOURCES") "AS IS". IDEAL AND/OR ITS LICENSORS DO NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE RESOURCES OR THAT SUCH RESOURCES WILL BE SUITABLE FOR YOUR APPLICATION. IDEAL HEREBY DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, OR NON-INFRINGEMENT.

You are only permitted to use the Resources and any products provided by iDEAL ("Products") in accordance with the operating parameters set forth in the Resources and iDEAL's standard terms and conditions made available at the time of order placement. Please note that the Resources are intended for skilled, technically-trained developers. You are solely responsible for, and iDEAL disclaims all responsibility and liability for: (a) choosing the Products and evaluating the suitability of such Products for the intended application, as well as determining if the information in the Resources is complete for your application; (b) designing, validating and testing the Products in your system; and (c) ensuring your application meets applicable safety, security, regulatory or other industry requirements and standards. iDEAL assumes no liability for any damage or malfunction resulting from improper handling of Products, or use of Products and Resources outside of the specified parameters. You are responsible for consulting the latest datasheet before placing orders.

iDEAL reserves the right to make corrections, modifications, enhancements, improvements and other change to or otherwise discontinue its Resources and Products in its sole discretion at any time without notice. All Products are sold subject to iDEAL's standard terms and conditions made available at the time of order placement.

Mailing Address:

iDEAL Semiconductor Devices, Inc.
116 Research Drive
Bethlehem, Pennsylvania, USA 18015
info@idealsemi.com