

SuperQ™ 200V N-Channel Power MOSFET

FEATURES

- Low $R_{DS(on)}$ in D2PAK-3L package rated to 175°C
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{sw} and E_{oss}
- Easier paralleling with $\pm 0.5V$ gate threshold

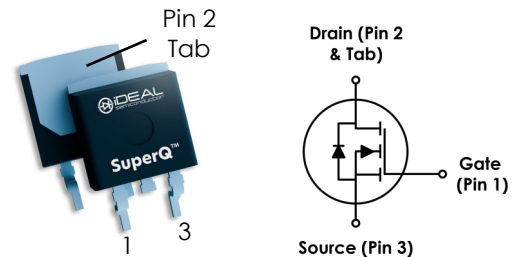
APPLICATIONS

- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

DESCRIPTION

Engineered for high-efficiency motor drives and SMPS, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust D2PAK-3L package. Featuring best-in-class $R_{DS(on)}$ and Q_{sw} , it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY



D2PAK-3L

Parameter	Value	Unit
$T_A = 25^\circ\text{C}$		
V_{DS}	200	V
$R_{DS(on),max}$	8.2	m Ω
I_D	115	A
Q_G	74	nC
Q_{sw}	4.9	nC
E_{oss}	3	μJ



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS20M8R0S1B	D2PAK-3L	iS20M8R0S1	13" 1,000pcs T&R

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	115	A
	Continuous drain current (silicon limited), $T_C = 100^\circ\text{C}$	81	
I_{DM}	Pulsed drain current	458	A
P_D	Power dissipation, $T_C = 25^\circ\text{C}$	250	W
T_J, T_{stg}	Operating junction, storage temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse $I_D = 59A$, $R_{GS} = 25\Omega$	176	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance - D2PAK-3L	-	-	0.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	$^\circ\text{C}/\text{W}$

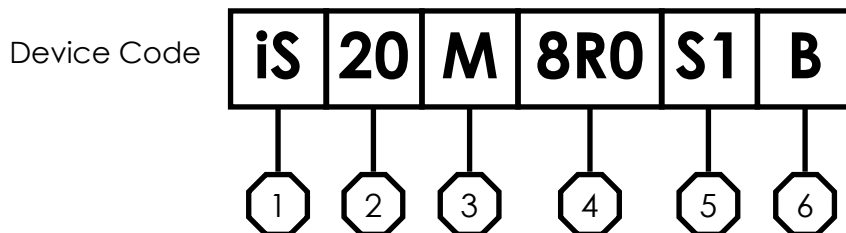
(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0V, I_D = 1mA$	200	-	-	V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0V, V_{DS} = 160V, T_J = 25^\circ\text{C}$	-	0.1	1	μA
		$V_{GS} = 0V, V_{DS} = 160V, T_J = 125^\circ\text{C}^{(2)}$	-	-	100	
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0V, V_{GS} = 20V$	-	20	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 213\mu\text{A}$	3.1	3.6	4.1	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 10V, I_D = 26A$	-	7.4	8.2	m Ω
g_{fs}	Transconductance	$V_{DS} = 10V, I_D = 26A$	49	97	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance ⁽²⁾	$V_{GS} = 0V, V_{DS} = 100V, f = 100\text{kHz}$	-	5,423	7,159	pF
C_{rss}	Reverse transfer capacitance ⁽²⁾		-	33	44	
C_{oss}	Output capacitance ⁽²⁾		-	206	268	
$C_{o(er)}$	Effective output capacitance	$V_{DS} = 0 \text{ to } 100V, V_{GS} = 0V$	-	598	-	
R_G	Series gate resistance	$f = 1\text{MHz}$	-	0.9	1.4	Ω
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 100V, V_{GS} = 10V, I_{DS} = 26A, R_{G,EXT} = 0\Omega$	-	TBD	-	ns
t_r	Rise time		-	TBD	-	
$t_{d(off)}$	Turn-off delay time		-	TBD	-	
t_f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q_G	Gate charge total ⁽²⁾	$V_{DS} = 100V, I_D = 26A, V_{GS} = 0 \text{ to } 10V$	-	74	96	nC
Q_{sw}	Switching charge ⁽³⁾		-	4.9	-	
Q_{gd}	Gate to drain charge ^{(2) (3)}		-	1.9	2.5	
$Q_{g(th)}$	Gate charge at threshold ⁽³⁾		-	17.3	-	
Q_{gs2}	Gate to source charge ⁽³⁾		-	2.9	-	
$V_{plateau}$	Gate plateau voltage		-	5.5	-	V
Q_{oss}	Output charge ⁽²⁾	$V_{DS} = 0 \text{ to } 100V, V_{GS} = 0V$	-	254	327	nC
E_{oss}	Capacitive stored energy		-	3.0	-	μJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 26A, V_{GS} = 0V$	-	1.1	1.3	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 100V, I_F = 26A,$	-	709	-	nC
t_{rr}	Reverse recovery time	$di/dt = 100A/\mu\text{s}$	-	147	-	ns

(2) Defined by design. Not subject to production test.

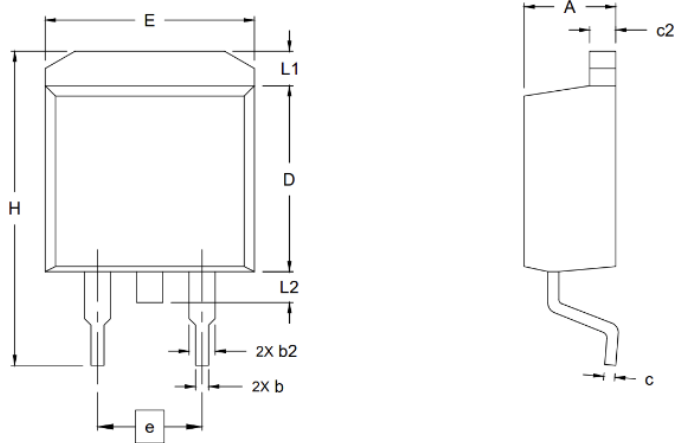
(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING



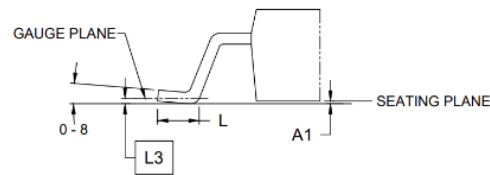
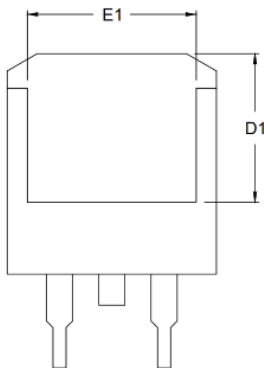
- 1 - iDEAL Semiconductor product
- 2 - Voltage rating divided by 10 (200V)
- 3 - M = N-Channel MOSFET, Standard Threshold
- 4 - Maximum drain-to-source resistance
- 5 - SuperQ™ Generation
- 6 - B = D2PAK-3L

D2PAK-3L Package Drawing



SYMBOL	MIN	MAX
A	4.07	4.83
A1	0.00	0.26
b	0.51	0.99
b2	1.14	1.78
c	0.38	0.74
c2	1.14	1.65
D	8.38	9.65
D1	6.86	--
E	9.65	10.67
E1	6.23	--
e	2.54 BSC	
H	14.61	15.88
L	1.78	2.80
L1	--	1.68
L2	--	1.78
L3	0.25 BSC	

- Notes:
1. All linear dimensions in millimeters
 2. Dimensions D and E do not include mold flash or protrusions



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