

SuperQ™ 200V N-Channel Power MOSFET

FEATURES

- Industry leading $R_{DS(on)}$ in TOLL package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{sw} and E_{oss}
- 175°C Industrial temperature rating

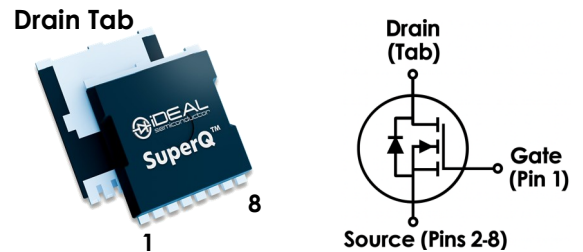
APPLICATIONS

- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

DESCRIPTION

Engineered for high-efficiency SMPS and motor drives, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust TOLL package. Featuring best-in-class $R_{DS(on)}$ and Q_{sw} , it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY



TOLL

Parameter	Value	Unit
$T_A = 25^\circ\text{C}$		
V_{DS}	200	V
$R_{DS(on),max}$	3.9	m Ω
I_D	191	A
Q_G	133	nC
Q_{sw}	7.3	nC
E_{oss}	4.1	μJ



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS20M3R9S1T	TOLL	iS20M3R9S1	13" 2,000pcs T&R

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	191	A
	Continuous drain current (silicon limited), $T_C = 100^\circ\text{C}$	135	
I_{DM}	Pulsed drain current	560	A
P_D	Power dissipation, $T_C = 25^\circ\text{C}$	314	W
T_J, T_{stg}	Operating junction, storage temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse $I_D = 60\text{A}$, $R_{GS} = 25\Omega$	788	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance - TOLL	-	-	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	$^\circ\text{C}/\text{W}$

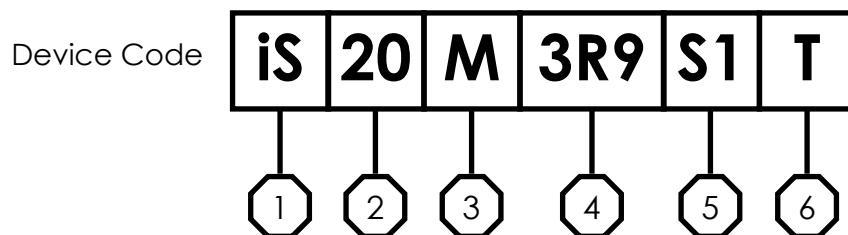
(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0V, I_D = 1mA$	200	-	-	V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0V, V_{DS} = 160V, T_J = 25^\circ\text{C}$	-	-	1	μA
		$V_{GS} = 0V, V_{DS} = 160V, T_J = 125^\circ\text{C}^{(2)}$	-	-	100	
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0V, V_{GS} = 20V$	-	-	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 300\mu\text{A}$	2.6	3.4	4.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 10V, I_D = 40A$	-	3.5	3.9	m Ω
g_{fs}	Transconductance	$V_{DS} = 10V, I_D = 40A$	40	80	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance ⁽²⁾	$V_{GS} = 0V, V_{DS} = 100V, f = 100\text{kHz}$	-	7,974	10,366	pF
C_{rss}	Reverse transfer capacitance ⁽²⁾		-	34	46	
C_{oss}	Output capacitance ⁽²⁾		-	267	347	
$C_{o(er)}$	Effective output capacitance	$V_{DS} = 0 \text{ to } 100V, V_{GS} = 0V$	-	805	-	
R_G	Series gate resistance	$f = 1\text{MHz}$	-	3.5	7	Ω
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 100V, V_{GS} = 10V, I_{DS} = 40A, R_{G,EXT} = 0\Omega$	-	TBD	-	ns
t_r	Rise time		-	TBD	-	
$t_{d(off)}$	Turn-off delay time		-	TBD	-	
t_f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q_G	Gate charge total ⁽²⁾	$V_{DS} = 100V, I_D = 40A, V_{GS} = 0 \text{ to } 10V$	-	133	172	nC
Q_{sw}	Switching charge ⁽³⁾		-	7.3	-	
Q_{gd}	Gate to drain charge ⁽²⁾		-	3.4	4.4	
$Q_{g(th)}$	Gate charge at threshold		-	25	-	
Q_{gs2}	Gate to source charge ⁽³⁾		-	3.9	-	
$V_{plateau}$	Gate plateau voltage		-	5.4	-	V
Q_{oss}	Output charge ⁽²⁾	$V_{DS} = 0 \text{ to } 100V, V_{GS} = 0V$	-	592	770	nC
E_{oss}	Capacitive stored energy		-	4.1	-	μJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 40A, V_{GS} = 0V$	-	0.8	1	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 100V, I_F = 40A,$	-	450	-	nC
t_{rr}	Reverse recovery time	$di/dt = 100A/\mu\text{s}$	-	110	-	ns

(2) Defined by design. Not subject to production test.

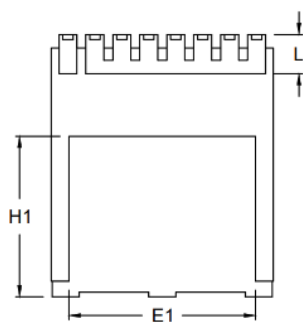
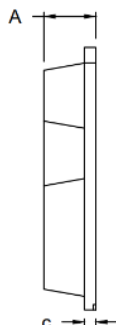
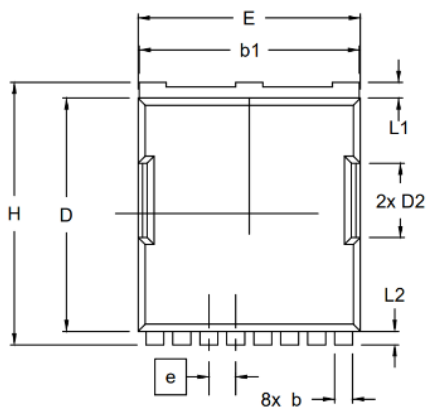
(3) Q_{sw} should be used for switching loss calculations. See Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING



- 1 - iDEAL Semiconductor product
- 2 - Voltage rating divided by 10 (200V)
- 3 - M = N-Channel MOSFET, Standard Threshold
- 4 - Maximum drain-to-source resistance
- 5 - SuperQ™ Generation
- 6 - T = TOLL

TOLL Package Drawing



SYMBOL	MIN	MAX
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
c	0.40	0.6
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.00
E1	7.90	8.60
e	1.20 BSC	
H	11.48	11.880
H1	6.75	7.43
L	1.40	2.10
L1	0.60	0.80
L2	0.500	0.700
θ	10° REF	

Notes:

1. All linear dimensions in millimeters

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