

SuperQ™ 200V N-Channel Power MOSFET

16mΩ, 62A, D2PAK-7L

FEATURES

- Low $R_{DS(on)}$ in D2PAK-7L package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{SW} and E_{OSS}
- Easier paralleling with $\pm 0.5V$ gate threshold tolerance

APPLICATIONS

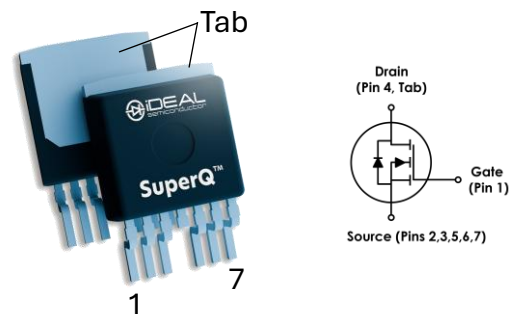
- Motor Control
- Boost Converters and SMPS Control FETs
- Class D Audio
- Battery Management Systems

PRODUCT SUMMARY

Parameter	Typ	Max	Unit
V_{DS}		200	V
$R_{DS(on)}$ @ 10V	14	16	mΩ
I_D		62	A
Q_G	29	37	nC
Q_{SW}	3		nC
E_{OSS}	1.5		μJ

DESCRIPTION

Engineered for SMPS and high-efficiency motor drives, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust D2PAK-7L package. Featuring low $R_{DS(on)}$ and industry leading Q_{SW} and E_{OSS} , it minimizes heat dissipation at both full and partial loads.



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS20M016S1H	D2PAK-7L	iS20M016S1H	1,000 pc Reel

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ($T_A = 25^\circ C$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), $T_C = 25^\circ C$	62	A
	Continuous drain current (silicon limited), $T_C = 100^\circ C$	44	
I_{DM}	Pulsed drain current	228	A
P_D	Power dissipation, $T_C = 25^\circ C$	150	W
T_J, T_{sg}	Operating junction, storage temperature	-55 to 175	$^\circ C$
E_{AS}	Avalanche energy, single pulse $I_D = 31A$, $R_{GS} = 25\Omega$	209	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ($T_A = 25^\circ C$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance – D2PAK-7L	-	-	1	$^\circ C/W$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	$^\circ C/W$
$R_{\theta JA}$	Junction-to-ambient thermal resistance, minimal footprint	-	-	62	$^\circ C/W$

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

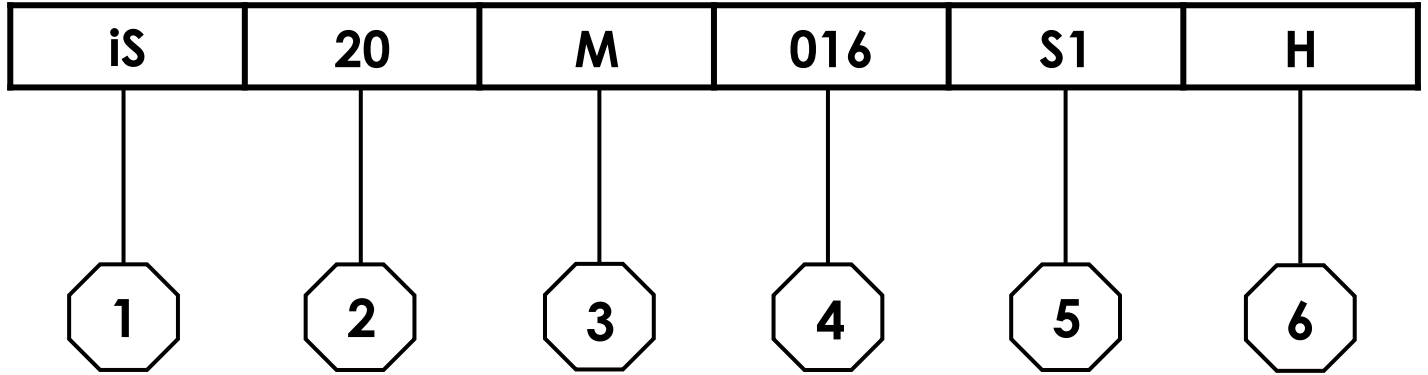
ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	200	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 160V, T _J = 25°C	-	0.05	1	μA
		V _{GS} = 0V, V _{DS} = 160V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	10	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 105μA	2.5	3	3.5	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 19A	-	14	16	mΩ
G _{fs}	Transconductance	V _{DS} = 10V, I _D = 19A	24	48	-	S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 100V, f = 100kHz	-	1,872	2433	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	11	15	
C _{oss}	Output capacitance ⁽²⁾		-	102	132	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 100V, V _{GS} = 0V	-	295	-	
R _G	Series gate resistance	f = 1MHz	-	1	2	Ω
t _{d(on)}	Turn-on delay time	V _{DS} = 100V, V _{GS} = 10V, I _{DS} = 19A, R _{G,EXT} = 0 Ω	-	TBD	-	ns
t _r	Rise time		-	TBD	-	
t _{d(off)}	Turn-off delay time		-	TBD	-	
t _f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q _g	Gate charge total ⁽²⁾	V _{DS} = 100V, I _D = 19A, V _{GS} = 0 to 10V	-	29	37	nC
Q _{sw}	Switching charge ⁽³⁾		-	3	-	
Q _{gd}	Gate to drain charge ⁽²⁾⁽³⁾		-	1.3	1.6	
Q _{g(th)}	Gate charge at threshold ⁽³⁾		-	9	-	
Q _{gs2}	Gate to source charge ⁽³⁾		-	1.7	-	
V _{plateau}	Gate plateau voltage		-	5	-	V
Q _{oss}	Output charge ⁽²⁾	V _{DS} = 0 to 100V, V _{GS} = 0V	-	125	163	nC
E _{oss}	Capacitive stored energy		-	1.5	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 19A, V _{GS} = 0V	-	1.0	1.2	V
Q _{rr}	Reverse recovery charge	V _{DS} = 100V, I _F = 19A,	-	446	-	nC
t _{rr}	Reverse recovery time	di/dt = 100A/μs	-	110	-	ns

(2) Defined by design. Not subject to production test

(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for definitions of gate charge. For more information, see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING

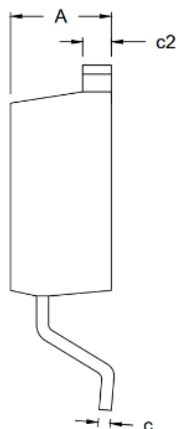
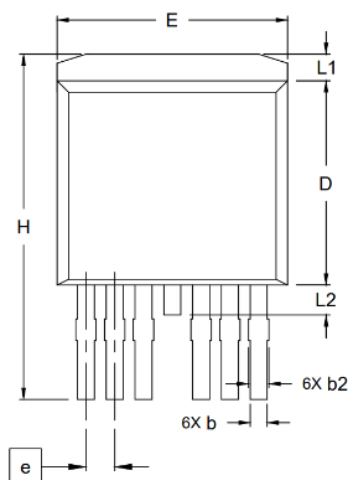
DEVICE CODE:



	— iDEAL Semiconductor product
	— Voltage rating divided by 10 (200V)
	— M = N-Channel MOSFET, Standard Threshold
	— Maximum drain-to-source resistance
	— SuperQ™ Generation
	— H = D2PAK-7L

Package Drawing

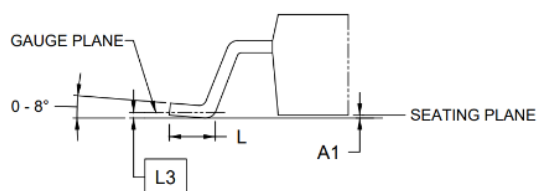
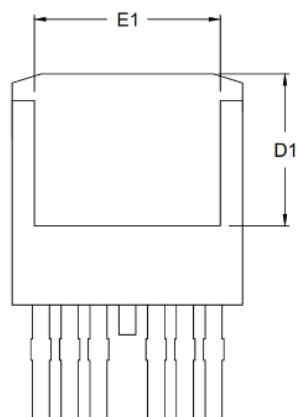
D2PAK-7L Package



SYMBOL	MIN	MAX
A	4.30	4.70
A1	--	0.25
b	0.50	0.85
b2	0.80	1.00
c	0.40	0.65
c2	1.20	1.40
D	8.50	9.40
D1	6.86	--
E	9.65	10.10
E1	6.50	--
e	1.27 BSC	
H	14.61	15.88
L	1.78	2.79
L1	--	1.60
L2	--	1.78
L3	0.25 BSC	

Notes:

1. All linear dimensions in millimeters
2. Dimensions D and E do not include mold flash or protrusions



Revision History

Revision History		
Version	Date	Comments
1.0	June 2026	Preliminary Rev 1.0

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design resources:



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