iS20M016S1B

SuperQ™ 200V N-Channel Power MOSFET

16mΩ, 62A, D2PAK-3L

FEATURES

- Low $R_{DS(on)}$ in D2PAK-3L package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{SW} and E_{OSS}
- Easier paralleling with ± 0.5V gate threshold tolerance

APPLICATIONS

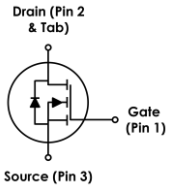
- Motor Control
- Boost Converters and SMPS Control FETs
- Class D Audio
- Battery Management Systems

PRODUCT SUMMARY

Parameter	Typ	Max	Unit
V_{DS}		200	V
$R_{DS(on)}$ @ 10V	14	16	mΩ
I_D		62	A
Q_G	29	37	nC
Q_{SW}	3		nC
E_{OSS}	1.5		µJ

DESCRIPTION

Engineered for SMPS and high-efficiency motor drives, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust D2PAK-3L package. Featuring low $R_{DS(on)}$ and industry leading Q_{SW} and E_{OSS}, it minimizes heat dissipation at both full and partial loads.



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS20M016S1B	D2PAK-3L	iS20M016S1B	1,000 pc Reel

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER (T_A = 25°C unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), TC = 25°C	62	A
	Continuous drain current (silicon limited), TC = 100°C	44	
I_{DM}	Pulsed drain current	228	A
P_D	Power dissipation, T_C = 25°C	150	W
T_J, T_{sg}	Operating junction, storage temperature	-55 to 175	°C
E_{AS}	Avalanche energy, single pulse I_D = 31A, R_{GS} = 25Ω	209	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER (T_A = 25°C unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance – D2PAK-3L	-	-	1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	-	-	50	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance, minimal footprint	-	-	62	°C/W

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

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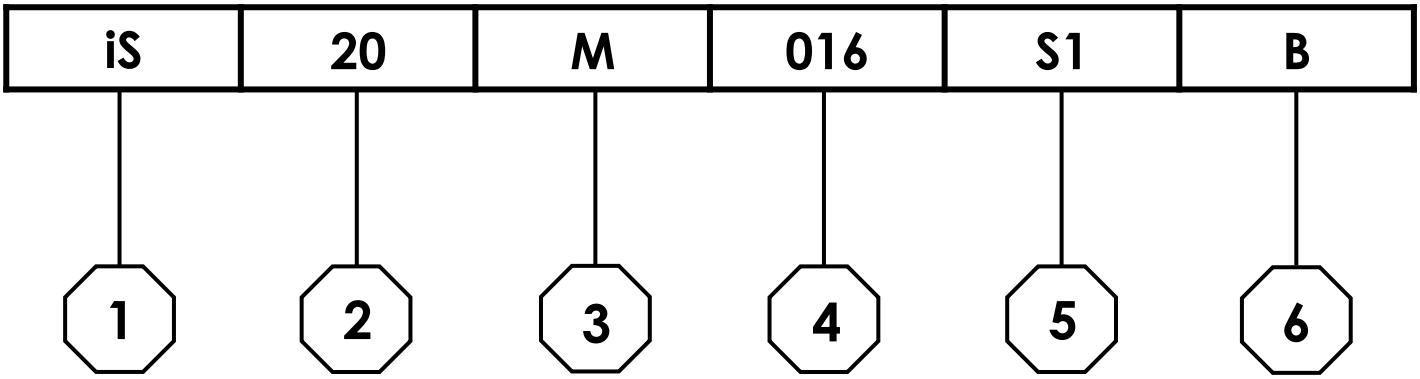
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 1mA	200	-	-	V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 160V, T_J = 25°C	-	0.05	1	µA
		V_{GS} = 0V, V_{DS} = 160V, T_J = 125°C(2)	-	-	100	
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V	-	10	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 105µA	2.5	3	3.5	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 10V, I_D = 19A	-	14	16	mΩ
G_{fs}	Transconductance	V_{DS} = 10V, I_D = 19A	24	48	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance (2)	V_{GS} = 0V, V_{DS} = 100V, f = 100kHz	-	1,872	2433	pF
C_{rss}	Reverse transfer capacitance (2)		-	11	15	
C_{oss}	Output capacitance (2)		-	102	132	
$C_{o(er)}$	Effective output capacitance	V_{DS} = 0 to 100V, V_{GS} = 0V	-	295	-	
R_G	Series gate resistance	f = 1MHz	-	1	2	Ω
$t_{d(on)}$	Turn-on delay time	V_{DS} = 100V, V_{GS} = 10V, I_{DS} = 19A, R_G,EXT = 0 Ω	-	TBD	-	ns
t_r	Rise time		-	TBD	-	
$t_{d(off)}$	Turn-off delay time		-	TBD	-	
t_f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q_g	Gate charge total (2)	V_{DS} = 100V, I_D = 19A, V_{GS} = 0 to 10V	-	29	37	nC
Q_{sw}	Switching charge (3)		-	3	-	
Q_{gd}	Gate to drain charge (2)(3)		-	1.3	1.6	
$Q_{g(th)}$	Gate charge at threshold (3)		-	9	-	
Q_{gs2}	Gate to source charge (3)		-	1.7	-	
$V_{plateau}$	Gate plateau voltage		-	5	-	V
Q_{oss}	Output charge (2)	V_{DS} = 0 to 100V, V_{GS} = 0V	-	125	163	nC
E_{oss}	Capacitive stored energy		-	1.5	-	µJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 19A, V_{GS} = 0V	-	1.0	1.2	V
Q_{rr}	Reverse recovery charge	V_{DS} = 100V, I_F = 19A, di/dt = 100A/µs	-	446	-	nC
t_{rr}	Reverse recovery time		-	110	-	ns

(2) Defined by design. Not subject to production test

(3) Q_{SW} should be used for switching loss calculations. See Figure 16 for definitions of gate charge. For more information, see Q_{SW} application note on www.idealsemi.com

DEVICE DECODER RING

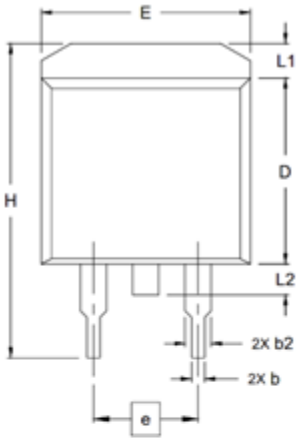
DEVICE CODE:



1	— iDEAL Semiconductor product
2	— Voltage rating divided by 10 (200V)
3	— M = N-Channel MOSFET, Standard Threshold
4	— Maximum drain-to-source resistance
5	— SuperQ™ Generation
6	— B = D2PAK-3L

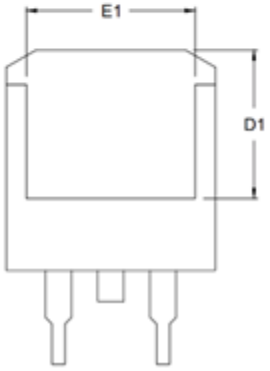
Package Drawing

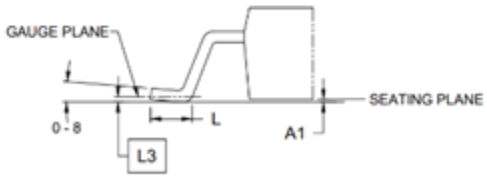
D2PAK-3L Package



SYMBOL	MIN	MAX
A	4.07	4.83
A1	0.00	0.26
b	0.51	0.99
b2	1.14	1.78
c	0.38	0.74
c2	1.14	1.65
D	8.38	9.65
D1	6.86	--
E	9.65	10.67
E1	6.23	--
e	2.54 BSC	
H	14.61	15.88
L	1.78	2.80
L1	--	1.68
L2	--	1.78
L3	0.25 BSC	

Notes:
1. All linear dimensions in millimeters
2. Dimensions D and E do not include mold flash or protrusions





Revision History

Revision History		
Version	**Date**	**Comments**
1.0	June 2026	Preliminary Rev 1.0

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