

SuperQ® 200V N-Channel Power MOSFET

16mΩ, 61A, PDFN 5x6

FEATURES

- Low $R_{DS(on)}$ in PDFN 5x6 package
- Logic level gate threshold tuned for 4.5V gate drive
- 100% UIS tested in production
- Low switching losses, Q_{SW} and E_{OSS}
- Easier paralleling with $\pm 0.5V$ gate threshold tolerance

APPLICATIONS

- Secondary side synchronous rectification
- Flyback and AC/DC adapters
- USB-C PD synchronous rectifier
- Bias supplies

PRODUCT SUMMARY

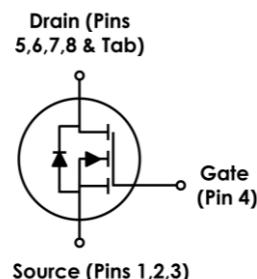
Parameter	Typ	Max	Unit
V_{DS}		200	V
$R_{DS(on)}$ @ 10V	14	16	mΩ
I_D		61	A
Q_G	29	37	nC
Q_{SW}	3.0		nC
E_{OSS}	1.5		μJ

DESCRIPTION

Engineered for synchronous rectification in flyback converters, this 200V SuperQ MOSFET combines low $R_{DS(on)}$ and low gate threshold voltage to minimize conduction losses and support efficient operation. Its compact PDFN 5x6 package enables high power density in space-constrained AC/DC power supplies.



PDFN 5x6



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS20L016S1C	PDFN 5x6	iS20M016S1	5ku Pcs Reel

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), $TC = 25^\circ\text{C}$	61	A
	Continuous drain current (silicon limited), $TC = 100^\circ\text{C}$	38	
I_{DM}	Pulsed drain current	222	
I_S	Continuous diode forward current, $TC = 25^\circ\text{C}$	61	
$I_{S, PULSE}$	Diode pulse current	222	
P_D	Power dissipation, $TC = 25^\circ\text{C}$	125	W
T_J, T_{SG}	Operating junction, storage temperature	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse $I_D = 31\text{A}$, $R_{GS} = 25\Omega$	209	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance – PDFN 5x6	-	-	1.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance, minimal footprint	-	-	62	$^\circ\text{C}/\text{W}$

(1) 40mm x 40mm x 1.5mm epoxy PCB FR4 with 6cm² (one-layer, 70μm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

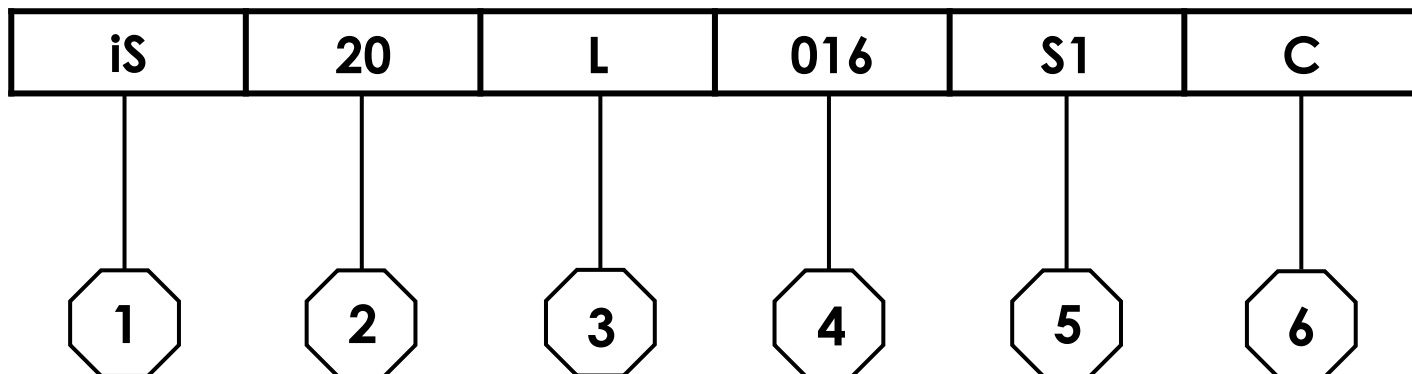
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	200	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 160V, T _J = 25°C	-	0.05	1.0	μA
		V _{GS} = 0V, V _{DS} = 160V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	10	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 105μA	1.5	2.0	2.5	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 19A	-	14	16	mΩ
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 4.5V, I _D = 10A	-	17.7	20	mΩ
g _{fs}	Transconductance	V _{DS} = 10V, I _D = 19A	24	48	-	S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 100V, f = 100kHz	-	1,872	2,433	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	11	15	
C _{oss}	Output capacitance ⁽²⁾		-	102	132	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 100V, V _{GS} = 0V	-	295	-	
R _g	Series gate resistance	f = 1MHz	-	1.0	2.0	Ω
T _{d(on)}	Turn-on delay time	V _{DS} = 100V, V _{GS} = 10V, I _{DS} = 19A, R _{G,EXT} = 0Ω	-	TBD	-	ns
T _r	Rise time		-	TBD	-	
T _{d(off)}	Turn-off delay time		-	TBD	-	
T _f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q _g	Gate charge total ⁽²⁾	V _{DS} = 100V, I _D = 19A, V _{GS} = 0 to 10V	-	29	37	nC
Q _{sw}	Switching charge ⁽³⁾		-	3.0	-	
Q _{gd}	Gate to drain charge ⁽²⁾⁽³⁾		-	1.3	1.6	
Q _{g(th)}	Gate charge at threshold ⁽³⁾		-	9.0	-	
Q _{gs2}	Gate to source charge ⁽³⁾		-	1.7	-	
V _{plateau}	Gate plateau voltage	V _{DS} = 0 to 100V, V _{GS} = 0V	-	3.0	-	V
Q _{oss}	Output charge ⁽²⁾		-	147	191	nC
E _{oss}	Capacitive stored energy		-	1.5	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 19A, V _{GS} = 0V	-	1.1	1.3	V
Q _{RR}	Reverse recovery charge	V _{DS} = 100V, I _F = 19A,	-	211	-	nC
t _{rr}	Reverse recovery time	di/dt = 100A/μs	-	87	-	ns

(2) Defined by design. Not subject to production test

(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for definitions of gate charge. For more information, see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING

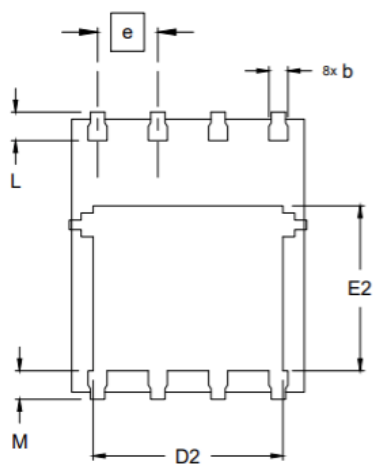
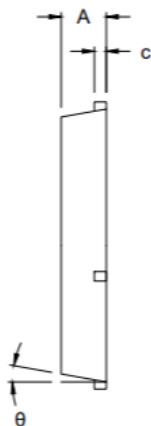
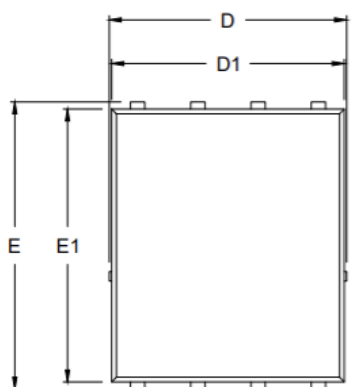
DEVICE CODE:



	— iDEAL Semiconductor product
	— Voltage rating divided by 10 (200V)
	— L = N-Channel MOSFET, Logic Level Threshold
	— Maximum drain-to-source resistance
	— SuperQ® Generation
	— C = PDFN 5x6

Package Drawing

PDFN 5x6 Package



SYMBOL	MIN	MAX
A	0.95	1.05
b	0.31	0.51
c	0.25 REF	
D	4.94	5.30
D1	4.80	5.1
D2	3.70	4.10
E	5.97	6.35
E1	5.67	6.10
E2	3.37	3.76
e	1.27 TYP	
L	0.51	0.71
M	0.51	0.73
θ	0°	10°

Revision History

Revision History		
Version	Date	Comments
Preliminary 1.0	October 2026	Preliminary Release

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design resources:



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