

SuperQ™ 150V N-Channel Power MOSFET

FEATURES

- Low $R_{DS(on)}$ in TOLT package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{sw} and E_{oss}
- Industrial rating to 175°C junction temperature

APPLICATIONS

- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

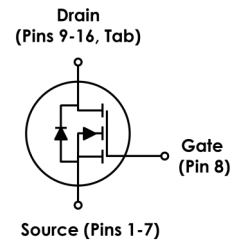
DESCRIPTION

Engineered for high-efficiency motor drives and SMPS, this 150V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust TOLT package. Featuring best-in-class $R_{DS(on)}$ and Q_{sw} , it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY



TOLT



Parameter	Value	Unit
$T_A = 25^\circ\text{C}$		
V_{DS}	150	V
$R_{DS(on),max}$	3.4	m Ω
I_D	182	A
Q_G	88	nC
Q_{sw}	8.9	nC
E_{oss}	1.7	μJ



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS15M3R4S1TC	TOLT	iS15M3R4S1	1,800pcs T&R

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	182	A
	Continuous drain current (silicon limited), $T_C = 100^\circ\text{C}$	129	
I_{DM}	Pulsed drain current	729	A
P_D	Power dissipation, $T_C = 25^\circ\text{C}$	250	W
T_J, T_{stg}	Operating junction, storage temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse $I_D = 43\text{A}$, $R_{GS} = 25\Omega$	450	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance - TOLT	-	-	0.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	$^\circ\text{C}/\text{W}$

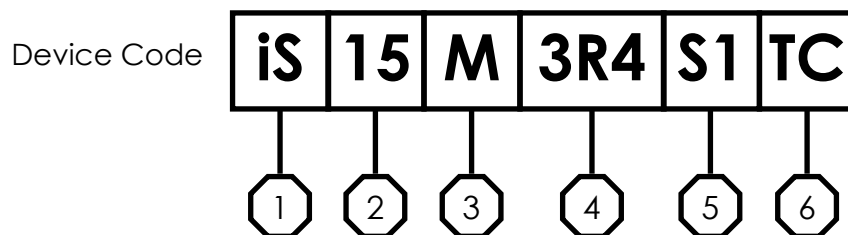
(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.







ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0V, I_D = 1mA$	150	-	-	V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0V, V_{DS} = 120V, T_J = 25^\circ\text{C}$	-	0.1	1	μA
		$V_{GS} = 0V, V_{DS} = 120V, T_J = 125^\circ\text{C}^{(2)}$	-	-	100	
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0V, V_{GS} = 20V$	-	30	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 231\mu\text{A}$	2.5	3.3	4.1	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 10V, I_D = 40A$	-	3.1	3.4	$m\Omega$
g_{fs}	Transconductance	$V_{DS} = 10V, I_D = 40A$	70	140	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance ⁽²⁾	$V_{GS} = 0V, V_{DS} = 75V, f = 100\text{kHz}$	-	5,373	6,985	pF
C_{rss}	Reverse transfer capacitance ⁽²⁾		-	67	88	
C_{oss}	Output capacitance ⁽²⁾		-	262	341	
$C_{o(er)}$	Effective output capacitance	$V_{DS} = 0 \text{ to } 75V, V_{GS} = 0V$	-	617	-	
R_G	Series gate resistance	$f = 1\text{MHz}$	-	1.2	1.8	Ω
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 75V, V_{GS} = 10V, I_{DS} = 40A,$ $R_{G,EXT} = 0\Omega$	-	TBD	-	ns
t_r	Rise time		-	TBD	-	
$t_{d(off)}$	Turn-off delay time		-	TBD	-	
t_f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q_G	Gate charge total ⁽²⁾	$V_{DS} = 75V, I_D = 40A,$ $V_{GS} = 0 \text{ to } 10V$	-	88	114	nC
Q_{sw}	Switching charge ⁽³⁾		-	8.9	-	
Q_{gd}	Gate to drain charge ^{(2) (3)}		-	5.5	7.2	
$Q_{g(th)}$	Gate charge at threshold ⁽³⁾		-	15.7	-	
Q_{gs2}	Gate to source charge ⁽³⁾		-	3.5	-	
$V_{plateau}$	Gate plateau voltage		-	5	-	V
Q_{oss}	Output charge ⁽²⁾	$V_{DS} = 0 \text{ to } 75V, V_{GS} = 0V$	-	241	313	nC
E_{oss}	Capacitive stored energy		-	1.7	-	μJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 40A, V_{GS} = 0V$	-	0.8	1.0	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 75V, I_F = 40A,$	-	216	-	nC
t_{rr}	Reverse recovery time	$di/dt = 100A/\mu\text{s}$	-	94	-	ns

(2) Defined by design. Not subject to production test.

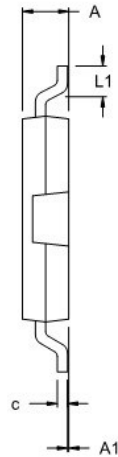
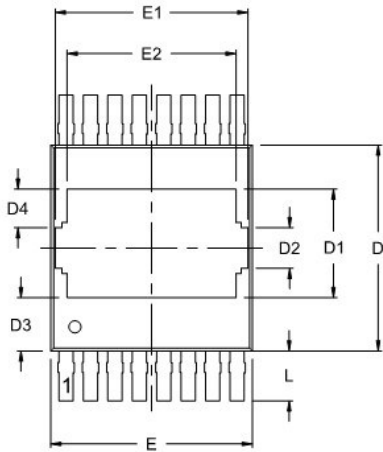
(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING



-  — iDEAL Semiconductor product
-  — Voltage rating divided by 10 (150V)
-  — M = N-Channel MOSFET, Standard Threshold
-  — Maximum drain-to-source resistance
-  — SuperQ™ Generation
-  — TC = TOLT

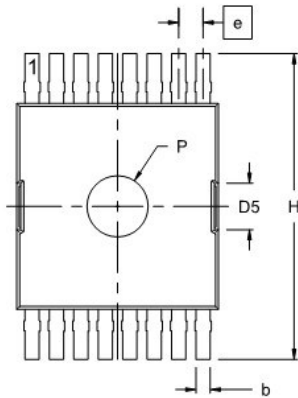
TOLT Package Drawing



SYMBOL	MIN	MAX
A	2.20	2.35
A1	0.01	0.11
b	0.60	0.85
c	0.45	0.65
D	10.00	10.30
D1	4.76	5.87
D2	1.80	2.20
D3	2.42	2.82
D4	1.33	2.44
D5	2.08	2.48
E	9.70	10.10
E1	9.26	9.66
E2	8.10	8.50
e	1.20 BSC	
H	14.80	15.20
L	2.25	2.65
L1	1.30	1.70
P	2.90	3.10

Notes:

1. All linear dimensions in millimeters



IMPORTANT NOTICE AND DISCLAIMER

IDEAL SEMICONDUCTOR DEVICES, INC. ("IDEAL") PROVIDES THE DATASHEET AND ALL SUPPORTING DESIGN RESOURCES, SAFETY INFORMATION, AND OTHER MATERIALS (THE "RESOURCES") "AS IS". IDEAL AND/OR ITS LICENSORS DO NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE RESOURCES OR THAT SUCH RESOURCES WILL BE SUITABLE FOR YOUR APPLICATION. IDEAL HEREBY DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, OR NON-INFRINGEMENT.

You are only permitted to use the Resources and any products provided by IDEAL ("Products") in accordance with the operating parameters set forth in the Resources and IDEAL's standard terms and conditions made available at the time of order placement. Please note that the Resources are intended for skilled, technically-trained developers. You are solely responsible for, and IDEAL disclaims all responsibility and liability for: (a) choosing the Products and evaluating the suitability of such Products for the intended application, as well as determining if the information in the Resources is complete for your application; (b) designing, validating and testing the Products in your system; and (c) ensuring your application meets applicable safety, security, regulatory or other industry requirements and standards. IDEAL assumes no liability for any damage or malfunction resulting from improper handling of Products, or use of Products and Resources outside of the specified parameters. You are responsible for consulting the latest datasheet before placing orders.

IDEAL reserves the right to make corrections, modifications, enhancements, improvements and other change to or otherwise discontinue its Resources and Products in its sole discretion at any time without notice. All Products are sold subject to IDEAL's standard terms and conditions made available at the time of order placement.

Mailing Address:

iDEAL Semiconductor Devices, Inc.
116 Research Drive
Bethlehem, Pennsylvania, USA 18015
info@idealsemi.com