iS15M3R4S1T

SuperQ™ 150V N-Channel Power MOSFET

FEATURES

- Low $R_{DS(on)}$ in TOLL package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{SW} and E_{OSS}
- Industrial rating to 175°C junction temperature

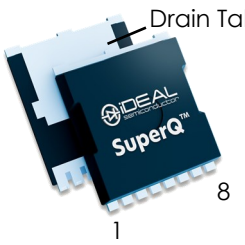
APPLICATIONS

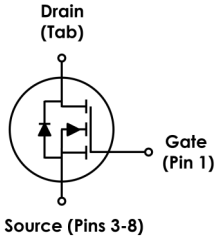
- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

DESCRIPTION

Engineered for high-efficiency motor drives and SMPS, this 150V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust TOLL package. Featuring best-in-class $R_{DS(on)}$ and Q_{SW}, it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY





TOLL

Parameter T_A = 25°C	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	3.4	mΩ
I_D	182	A
Q_G	88	nC
Q_{SW}	8.9	nC
E_{OSS}	1.7	µJ

ORDERING INFORMATION			
Part Number	**Package**	**Marking**	**Packaging**
iS15M3R4S1T	TOLL	iS15M3R4S1	13" 2,000pcs T&R

ABSOLUTE MAXIMUM RATINGS			
SYMBOL	**PARAMETER** (T_A = 25°C unless otherwise specified)	**VALUE**	**UNIT**
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), T_C = 25°C	182	A
	Continuous drain current (silicon limited), T_C = 100°C	129	
I_{DM}	Pulsed drain current	729	A
P_D	Power dissipation, T_C = 25°C	250	W
T_J, T_{stg}	Operating junction, storage temperature	-55 to 175	°C
E_{AS}	Avalanche energy, single pulse I_D = 43A, R_{GS} = 25Ω	450	mJ

THERMAL CHARACTERISTICS					
SYMBOL	**PARAMETER** (T_A = 25°C unless otherwise specified)	**VALUE**			**UNIT**
		MIN	**TYP**	**MAX**	
$R_{\theta JC}$	Junction-to-case thermal resistance - TOLL	-	-	0.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	-	-	50	°C/W

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

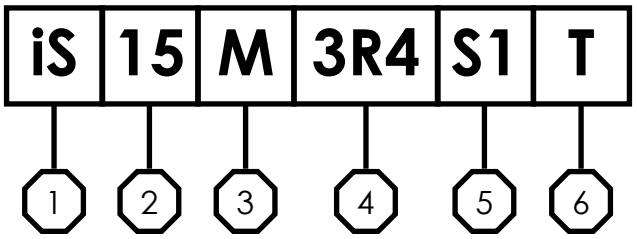
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 1mA	150	-	-	V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 120V, T_J = 25°C	-	0.1	1	µA
		V_{GS} = 0V, V_{DS} = 120V, T_J = 125°C (2)	-	-	100	
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V	-	30	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 231µA	2.5	3.3	4.1	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 10V, I_D = 40A	-	3.1	3.4	mΩ
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 40A	70	140	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance (2)	V_{GS} = 0V, V_{DS} = 75V, f = 100kHz	-	5,373	6,985	pF
C_{rss}	Reverse transfer capacitance (2)		-	67	88	
C_{oss}	Output capacitance (2)		-	262	341	
$C_{o(er)}$	Effective output capacitance	V_{DS} = 0 to 75V, V_{GS} = 0V	-	617	-	
R_G	Series gate resistance	f = 1MHz	-	1.2	1.8	Ω
$t_{d(on)}$	Turn-on delay time	V_{DS} = 75V, V_{GS} = 10V, I_{DS} = 40A, $R_{G,EXT}$ = 0 Ω	-	TBD	-	ns
t_r	Rise time		-	TBD	-	
$t_{d(off)}$	Turn-off delay time		-	TBD	-	
t_f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q_g	Gate charge total (2)	V_{DS} = 75V, I_D = 40A, V_{GS} = 0 to 10V	-	88	114	nC
Q_{sw}	Switching charge (3)		-	8.9	-	
Q_{gd}	Gate to drain charge (2) (3)		-	5.5	7.2	
$Q_{g(th)}$	Gate charge at threshold (3)		-	15.7	-	
Q_{gs2}	Gate to source charge (3)		-	3.5	-	
$V_{plateau}$	Gate plateau voltage		-	5	-	V
Q_{oss}	Output charge (2)	V_{DS} = 0 to 75V, V_{GS} = 0V	-	241	313	nC
E_{oss}	Capacitive stored energy		-	1.7	-	µJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 40A, V_{GS} = 0V	-	0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS} = 75V, I_F = 40A, di/dt = 100A/µs	-	216	-	nC
t_{rr}	Reverse recovery time		-	94	-	ns

(2) Defined by design. Not subject to production test.

(3) Q_{SW} should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING

Device Code



1 – iDEAL Semiconductor product

2 – Voltage rating divided by 10 (150V)

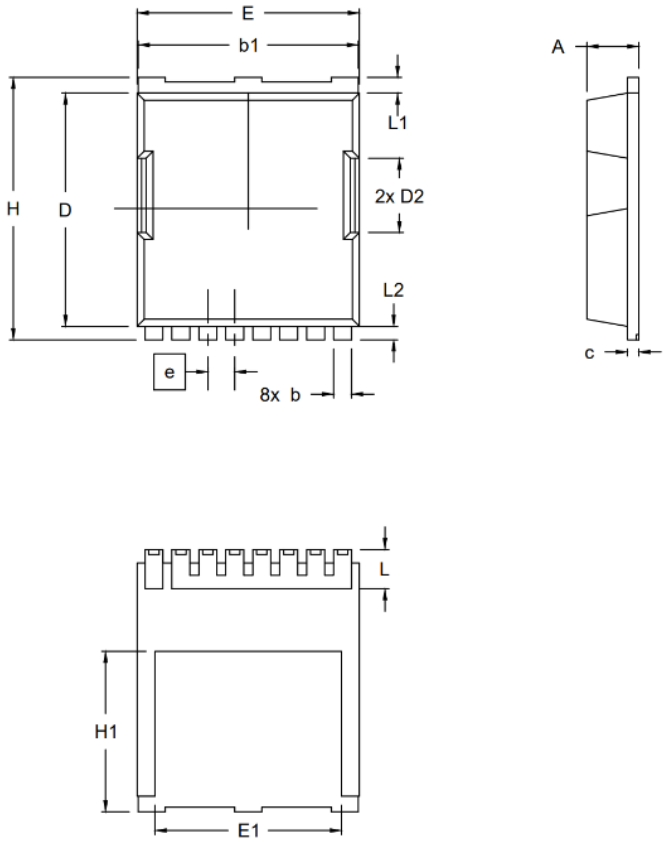
3 – M = N-Channel MOSFET, Standard Threshold

4 – Maximum drain-to-source resistance

5 – SuperQ™ Generation

6 – T = TOLL

TOLL Package Drawing



SYMBOL	MIN	MAX
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
c	0.40	0.6
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.00
E1	7.90	8.60
e	1.20 BSC	
H	11.48	11.880
H1	6.75	7.43
L	1.40	2.10
L1	0.60	0.80
L2	0.500	0.700
θ	10° REF	

Notes:
1. All linear dimensions in millimeters

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