

SuperQ™ 150V N-Channel Power MOSFET

FEATURES

- Low $R_{DS(on)}$ in D2PAK-7L package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{sw} and E_{oss}
- Industrial rating to 175°C junction temperature

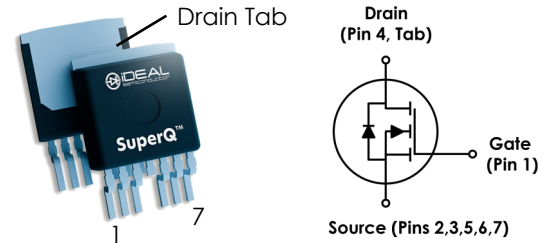
APPLICATIONS

- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

DESCRIPTION

Engineered for high-efficiency motor drives and SMPS, this 150V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust D2PAK-7L package. Featuring best-in-class $R_{DS(on)}$ and Q_{sw} , it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY



D2PAK-7L

Parameter	Value	Unit
$T_A = 25^\circ\text{C}$		
V_{DS}	150	V
$R_{DS(on),max}$	3.4	m Ω
I_D	182	A
Q_G	88	nC
Q_{sw}	8.9	nC
E_{oss}	1.7	μJ



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS15M3R4S1H	D2PAK-7L	iS15M3R4S1	2,000pcs T&R

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	182	A
	Continuous drain current (silicon limited), $T_C = 100^\circ\text{C}$	129	
I_{DM}	Pulsed drain current	729	A
P_D	Power dissipation, $T_C = 25^\circ\text{C}$	250	W
T_J, T_{stg}	Operating junction, storage temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse $I_D = 43\text{A}$, $R_{GS} = 25\Omega$	450	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance - D2PAK-7L	-	-	0.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	-	-	50	$^\circ\text{C}/\text{W}$

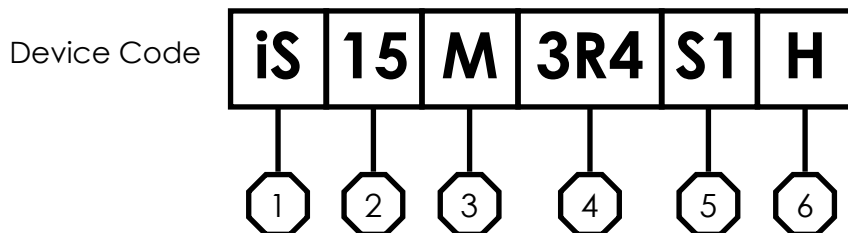
(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.







ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	150	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 120V, T _J = 25°C	-	0.1	1	μA
		V _{GS} = 0V, V _{DS} = 120V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	30	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 231μA	2.5	3.3	4.1	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 40A	-	3.1	3.4	mΩ
g _{fs}	Transconductance	V _{DS} = 10V, I _D = 40A	70	140	-	S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 75V, f = 100kHz	-	5,373	6,985	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	67	88	
C _{oss}	Output capacitance ⁽²⁾		-	262	341	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 75V, V _{GS} = 0V	-	617	-	
R _G	Series gate resistance	f = 1MHz	-	1.2	1.8	Ω
t _{d(on)}	Turn-on delay time	V _{DS} = 75V, V _{GS} = 10V, I _{DS} = 40A, R _{G,EXT} = 0 Ω	-	TBD	-	ns
t _r	Rise time		-	TBD	-	
t _{d(off)}	Turn-off delay time		-	TBD	-	
t _f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q _G	Gate charge total ⁽²⁾	V _{DS} = 75V, I _D = 40A, V _{GS} = 0 to 10V	-	88	114	nC
Q _{sw}	Switching charge ⁽³⁾		-	8.9	-	
Q _{Gd}	Gate to drain charge ^{(2) (3)}		-	5.5	7.2	
Q _{G(th)}	Gate charge at threshold ⁽³⁾		-	15.7	-	
Q _{Gs2}	Gate to source charge ⁽³⁾		-	3.5	-	
V _{plateau}	Gate plateau voltage		-	5	-	V
Q _{oss}	Output charge ⁽²⁾	V _{DS} = 0 to 75V, V _{GS} = 0V	-	241	313	nC
E _{oss}	Capacitive stored energy		-	1.7	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 40A, V _{GS} = 0V	-	0.8	1.0	V
Q _{rr}	Reverse recovery charge	V _{DS} = 75V, I _F = 40A,	-	216	-	nC
t _{rr}	Reverse recovery time	di/dt = 100A/μs	-	94	-	ns

(2) Defined by design. Not subject to production test.

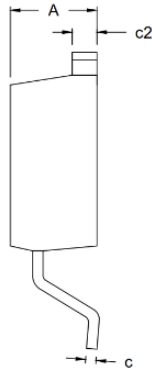
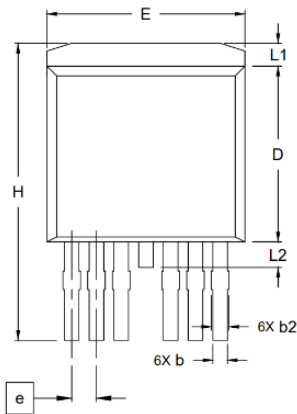
(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING



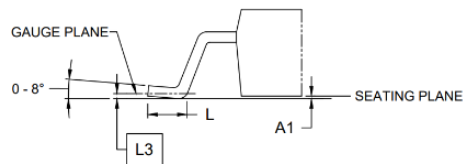
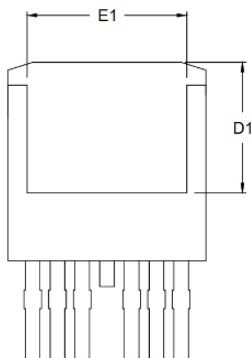
-  1 — iDEAL Semiconductor product
-  2 — Voltage rating divided by 10 (150V)
-  3 — M = N-Channel MOSFET, Standard Threshold
-  4 — Maximum drain-to-source resistance
-  5 — SuperQ™ Generation
-  6 — H = D2PAK-7L

D2PAK-7L Package Drawing



SYMBOL	MIN	MAX
A	4.30	4.70
A1	--	0.25
b	0.50	0.85
b2	0.80	1.00
c	0.40	0.65
c2	1.20	1.40
D	8.50	9.40
D1	6.86	--
E	9.65	10.10
E1	6.50	--
e	1.27 BSC	
H	14.61	15.88
L	1.78	2.79
L1	--	1.60
L2	--	1.78
L3	0.25 BSC	

- Notes:
1. All linear dimensions in millimeters
 2. Dimensions D and E do not include mold flash or protrusions



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