

## SuperQ™ 150V N-Channel Power MOSFET

### FEATURES

- Low  $R_{DS(on)}$  in D2PAK-3L package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses,  $Q_{sw}$  and  $E_{oss}$
- Industrial rating to 175°C junction temperature

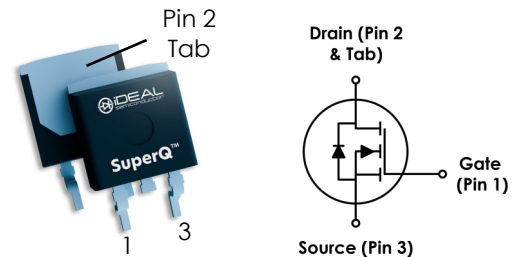
### APPLICATIONS

- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

### DESCRIPTION

Engineered for high-efficiency motor drives and SMPS, this 150V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust D2PAK-3L package. Featuring best-in-class  $R_{DS(on)}$  and  $Q_{sw}$ , it minimizes heat dissipation at both full and partial loads.

### PRODUCT SUMMARY



### D2PAK-3L

Parameter	Value	Unit
$T_A = 25^\circ\text{C}$		
$V_{DS}$	150	V
$R_{DS(on),max}$	3.4	m $\Omega$
$I_D$	182	A
$Q_G$	88	nC
$Q_{sw}$	8.9	nC
$E_{oss}$	1.7	$\mu\text{J}$



### ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS15M3R4S1B	D2PAK-3L	iS15M3R4S1	1,000pcs T&R

### ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ( $T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
$V_{GS}$	Gate-to-source voltage	$\pm 20$	V
$I_D$	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	182	A
	Continuous drain current (silicon limited), $T_C = 100^\circ\text{C}$	129	
$I_{DM}$	Pulsed drain current	729	A
$P_D$	Power dissipation, $T_C = 25^\circ\text{C}$	250	W
$T_J, T_{stg}$	Operating junction, storage temperature	-55 to 175	$^\circ\text{C}$
$E_{AS}$	Avalanche energy, single pulse $I_D = 43\text{A}$ , $R_{GS} = 25\Omega$	450	mJ

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ( $T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance - D2PAK-3L	-	-	0.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	-	-	50	$^\circ\text{C}/\text{W}$

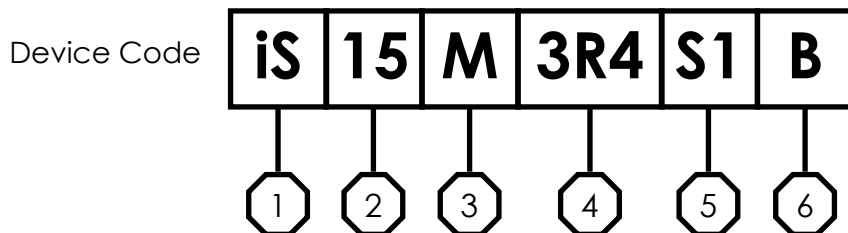
(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.







<b>ELECTRICAL CHARACTERISTICS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
<b>STATIC CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-to-source voltage	$V_{GS} = 0V, I_D = 1mA$	150	-	-	V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0V, V_{DS} = 120V, T_J = 25^\circ\text{C}$	-	0.1	1	$\mu\text{A}$
		$V_{GS} = 0V, V_{DS} = 120V, T_J = 125^\circ\text{C}^{(2)}$	-	-	100	
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0V, V_{GS} = 20V$	-	30	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 231\mu\text{A}$	2.5	3.3	4.1	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 10V, I_D = 40A$	-	3.1	3.4	$m\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 10V, I_D = 40A$	70	140	-	S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance <sup>(2)</sup>	$V_{GS} = 0V, V_{DS} = 75V, f = 100kHz$	-	5,373	6,985	$\text{pF}$
$C_{rss}$	Reverse transfer capacitance <sup>(2)</sup>		-	67	88	
$C_{oss}$	Output capacitance <sup>(2)</sup>		-	262	341	
$C_{o(er)}$	Effective output capacitance	$V_{DS} = 0 \text{ to } 75V, V_{GS} = 0V$	-	617	-	
$R_G$	Series gate resistance	$f = 1MHz$	-	1.2	1.8	$\Omega$
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 75V, V_{GS} = 10V, I_{DS} = 40A,$ $R_{G,EXT} = 0\Omega$	-	TBD	-	ns
$t_r$	Rise time		-	TBD	-	
$t_{d(off)}$	Turn-off delay time		-	TBD	-	
$t_f$	Fall time		-	TBD	-	
<b>GATE CHARGE CHARACTERISTICS</b>						
$Q_G$	Gate charge total <sup>(2)</sup>	$V_{DS} = 75V, I_D = 40A,$ $V_{GS} = 0 \text{ to } 10V$	-	88	114	nC
$Q_{sw}$	Switching charge <sup>(3)</sup>		-	8.9	-	
$Q_{gd}$	Gate to drain charge <sup>(2) (3)</sup>		-	5.5	7.2	
$Q_{g(th)}$	Gate charge at threshold <sup>(3)</sup>		-	15.7	-	
$Q_{gs2}$	Gate to source charge <sup>(3)</sup>		-	3.5	-	
$V_{plateau}$	Gate plateau voltage		-	5	-	V
$Q_{oss}$	Output charge <sup>(2)</sup>	$V_{DS} = 0 \text{ to } 75V, V_{GS} = 0V$	-	241	313	nC
$E_{oss}$	Capacitive stored energy		-	1.7	-	$\mu\text{J}$
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 40A, V_{GS} = 0V$	-	0.8	1.0	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 75V, I_F = 40A,$	-	216	-	nC
$t_{rr}$	Reverse recovery time	$di/dt = 100A/\mu\text{s}$	-	94	-	ns

(2) Defined by design. Not subject to production test.

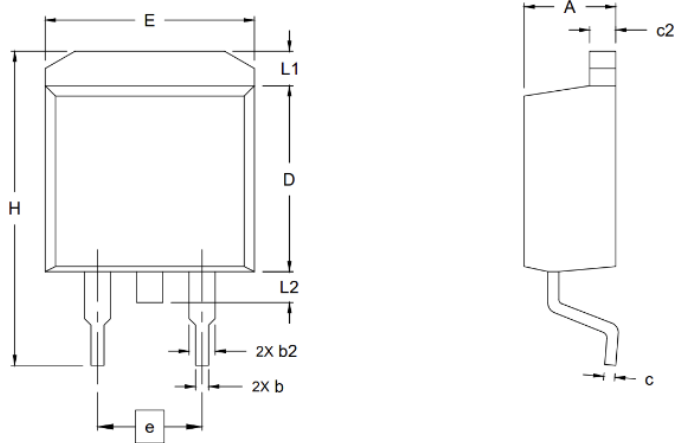
(3)  $Q_{sw}$  should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see  $Q_{sw}$  application note on [www.idealsemi.com](http://www.idealsemi.com)

## DEVICE DECODER RING



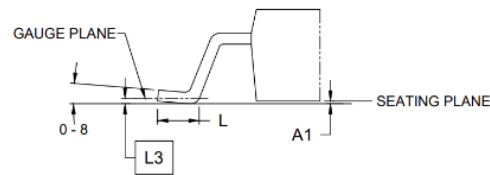
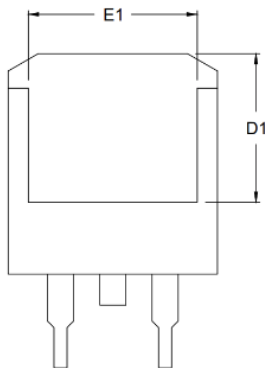
-  — iDEAL Semiconductor product
-  — Voltage rating divided by 10 (150V)
-  — M = N-Channel MOSFET, Standard Threshold
-  — Maximum drain-to-source resistance
-  — SuperQ™ Generation
-  — B = D2PAK-3L

## D2PAK-3L Package Drawing



SYMBOL	MIN	MAX
A	4.07	4.83
A1	0.00	0.26
b	0.51	0.99
b2	1.14	1.78
c	0.38	0.74
c2	1.14	1.65
D	8.38	9.65
D1	6.86	--
E	9.65	10.67
E1	6.23	--
e	2.54 BSC	
H	14.61	15.88
L	1.78	2.80
L1	--	1.68
L2	--	1.78
L3	0.25 BSC	

- Notes:
1. All linear dimensions in millimeters
  2. Dimensions D and E do not include mold flash or protrusions



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Mailing Address:

iDEAL Semiconductor Devices, Inc.  
116 Research Drive  
Bethlehem, Pennsylvania, USA 18015  
[info@idealsemi.com](mailto:info@idealsemi.com)