

SuperQ™ 150V N-Channel Power MOSFET

FEATURES

- Low on-resistance, $R_{DS(on)}$
- N-channel, logic level threshold
- Ultra low energy stored, E_{oss}
- Low reverse recovery time T_{rr} and Q_{rr}
- 100% UIS tested in production

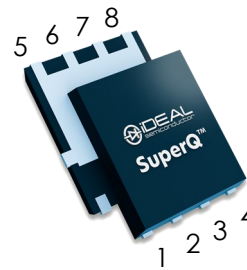
APPLICATIONS

- Synchronous rectification with 5V gate drive
- SMPS control FETs
- Motor control

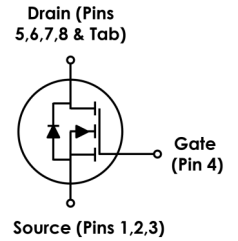
DESCRIPTION

This 150 V SuperQ™ power MOSFET, with a typical $R_{DS(ON)}$ of $7.3\text{ m}\Omega_{TYP}$, is designed for synchronous rectification using 5 V gate drive. Optimized for low Q_{RR} , Q_G , and E_{OSS} , the device reduces reverse recovery and switching losses, supporting high-frequency operation and improved efficiency in DC-DC conversion stages.

PRODUCT SUMMARY



PDFN 5x6mm



Parameter	Value	Unit
$T_A = 25^\circ\text{C}$		
V_{DS}	150	V
$R_{DS(on),max}$	8.8	m Ω
I_D	80	A
Q_G	40	nC
Q_{sw}	3	nC
E_{oss}	0.8	μJ



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS15L8R8S1C	PDFN 5X6	iS5LP02C (engr) iS15L8R8S1 (prod)	13" 5,000pcs T&R

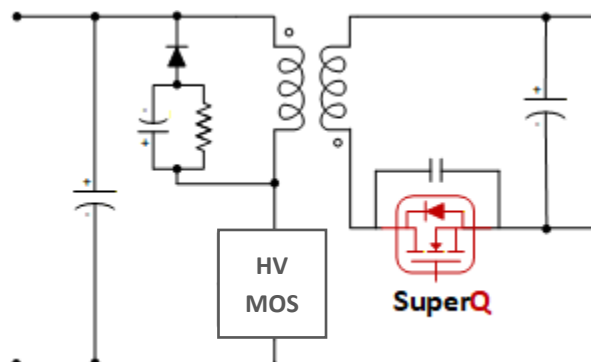


Figure 1: Example Application - Flyback converter with SuperQ synchronous rectifier

ABSOLUTE MAXIMUM RATINGS			
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE	UNIT
V _{GS}	Gate-to-source voltage	± 16	V
I _D	Continuous drain current (silicon limited), T _C = 25°C	80	A
	Continuous drain current (silicon limited), T _C = 100°C	51	
I _{DM}	Pulsed drain current	288	A
P _D	Power dissipation, T _C = 25°C	125	W
T _J , T _{stg}	Operating junction, storage temperature	-55 to 150	°C
E _{AS}	Avalanche energy, single pulse I _D = 9.4A, R _{GS} = 25Ω	446	mJ

THERMAL CHARACTERISTICS					
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
R _{θJC}	Junction-to-case thermal resistance - PDFN 5x6	-	-	1	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	°C/W

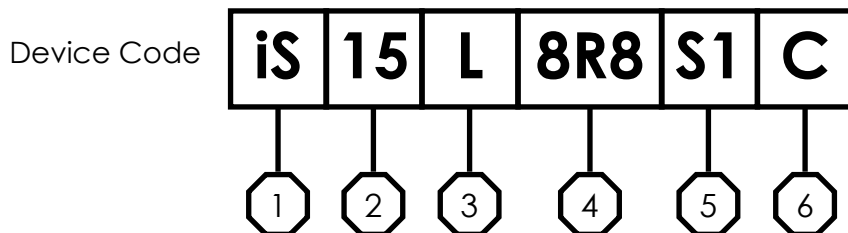
(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0V, I_D = 1mA$	150	-	-	V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0V, V_{DS} = 120V, T_J = 25^\circ\text{C}$	-	0.1	1	μA
		$V_{GS} = 0V, V_{DS} = 120V, T_J = 125^\circ\text{C}^{(2)}$	-	-	100	
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0V, V_{GS} = 20V$	-	1	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 94\mu\text{A}$	1.3	1.8	2.3	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 10V, I_D = 20A$	-	7.3	8.8	$\text{m}\Omega$
		$V_{GS} = 4.5V, I_D = 10A$	-	8.4	10.9	$\text{m}\Omega$
g_{fs}	Transconductance	$V_{DS} = 10V, I_D = 20A$	37	74	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance ⁽²⁾	$V_{GS} = 0V, V_{DS} = 75V, f = 100\text{kHz}$	-	2,313	3,007	pF
C_{rss}	Reverse transfer capacitance ⁽²⁾		-	21	27	
C_{oss}	Output capacitance ⁽²⁾		-	103	133	
$C_{o(er)}$	Effective output capacitance	$V_{DS} = 0 \text{ to } 75V, V_{GS} = 0V$	-	139	-	
R_G	Series gate resistance	$f = 1\text{MHz}$	-	0.8	1.2	Ω
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 75V, V_{GS} = 10V, I_{DS} = 20A,$ $R_{G,EXT} = 0\Omega$	-	TBD	-	ns
t_r	Rise time		-	TBD	-	
$t_{d(off)}$	Turn-off delay time		-	TBD	-	
t_f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q_g	Gate charge total ⁽²⁾	$V_{DS} = 75V, I_D = 20A,$ $V_{GS} = 0 \text{ to } 10V$	-	40	52	nC
Q_{sw}	Switching charge ⁽³⁾		-	3	-	
Q_{gd}	Gate to drain charge ⁽²⁾		-	1.5	4.2	
$Q_{g(th)}$	Gate charge at threshold ⁽³⁾		-	4.9	-	
Q_{gs2}	Gate to source charge ⁽³⁾		-	1.5	-	
$V_{plateau}$	Gate plateau voltage		-	3.7	-	V
Q_{oss}	Output charge ⁽²⁾	$V_{DS} = 0 \text{ to } 75V, V_{GS} = 0V$	-	102	118	nC
E_{oss}	Capacitive stored energy		-	0.8	-	μJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 20A, V_{GS} = 0V$	-	0.8	0.9	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 75V, I_F = 20A, di/dt = 100A/\mu\text{s}$	-	58	-	nC
t_{rr}	Reverse recovery time		-	61	-	ns

(2) Defined by design. Not subject to production test.

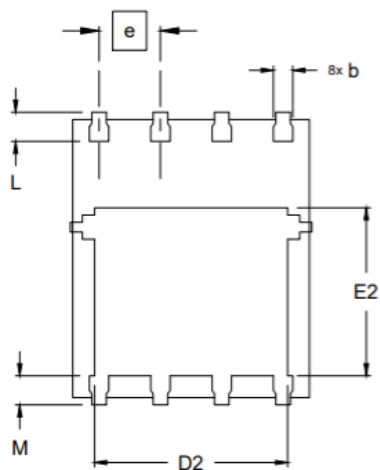
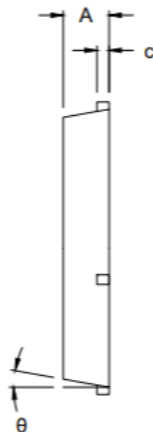
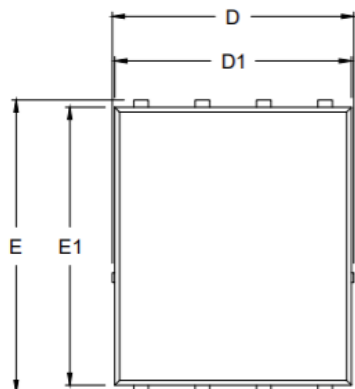
(3) Q_{sw} should be used for switching loss calculations. For more information see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING



- 1 - iDEAL Semiconductor product
- 2 - Voltage rating divided by 10 (150V)
- 3 - L = N-Channel MOSFET, Logic Level Threshold
- 4 - Maximum drain-to-source resistance
- 5 - SuperQ™ Generation
- 6 - C = PDFN 5x6mm

PDFN 5x6mm



SYMBOL	MIN	MAX
A	0.95	1.05
b	0.31	0.51
c	0.25 REF	
D	4.94	5.30
D1	4.80	5.1
D2	3.70	4.10
E	5.97	6.35
E1	5.67	6.10
E2	3.37	3.76
e	1.27 TYP	
L	0.51	0.71
M	0.51	0.73
θ	0°	10°

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Mailing Address:

iDEAL Semiconductor Devices, Inc.
116 Research Drive
Bethlehem, Pennsylvania, USA 18015
info@idealsemi.com