SuperQ™ 150V N-Channel Power MOSFET

FEATURES

- Low on-resistance, $R_{DS(on)}$
- N-channel, logic level threshold
- Ultra low energy stored, E_{OSS}
- Low reverse recovery time T_{rr} and Q_{rr}
- 100% UIS tested in production

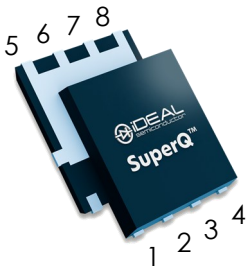
APPLICATIONS

- Synchronous rectification with 5V gate drive
- SMPS control FETs
- Motor control

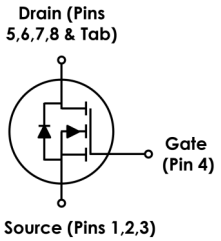
DESCRIPTION

This 150 V SuperQ™ power MOSFET, with a typical $R_{DS(ON)}$ of 5.1 $m\Omega_{TYP}$, is designed for synchronous rectification using 5 V gate drive. Optimized for low Q_{RR}, Q_G, and E_{OSS}, the device reduces reverse recovery and switching losses, supporting high-frequency operation and improved efficiency in DC-DC conversion stages.

PRODUCT SUMMARY



PDFN 5x6mm



Parameter T_A = 25°C	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	6.0	mΩ
I_D	126	A
Q_G	48	nC
Q_{SW}	4.9	nC
E_{OSS}	1	µJ

ORDERING INFORMATION			
Part Number	**Package**	**Marking**	**Packaging**
iS15L6R0S1C	PDFN 5X6	iS5LP00C (engr) iS15L6R0S1 (prod)	13" 5,000pcs T&R

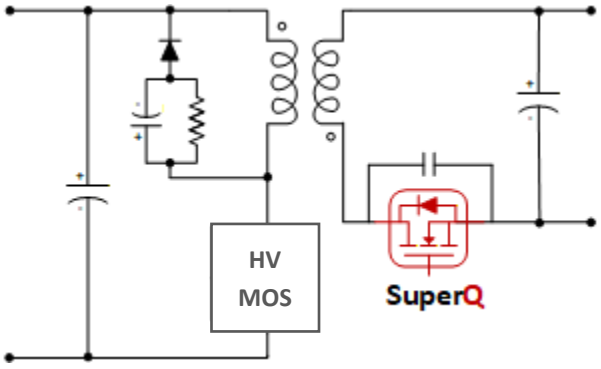


Figure 1: Example Application - Flyback converter with SuperQ synchronous rectifier

ABSOLUTE MAXIMUM RATINGS			
SYMBOL	**PARAMETER** (T_A = 25°C unless otherwise specified)	**VALUE**	**UNIT**
V_{GS}	Gate-to-source voltage	± 16	V
I_D	Continuous drain current (silicon limited), T_C = 25°C	126	A
	Continuous drain current (silicon limited), T_C = 100°C	79	
I_{DM}	Pulsed drain current	435	A
P_D	Power dissipation, T_C = 25°C	208	W
T_J, T_{stg}	Operating junction, storage temperature	-55 to 150	°C
E_{AS}	Avalanche energy, single pulse I_D = 11.3A, R_{GS} = 25Ω	641	mJ

THERMAL CHARACTERISTICS					
SYMBOL	**PARAMETER** (T_A = 25°C unless otherwise specified)	**VALUE**			**UNIT**
		MIN	**TYP**	**MAX**	
$R_{\theta JC}$	Junction-to-case thermal resistance - PDFN 5x6	-	-	0.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	-	-	50	°C/W

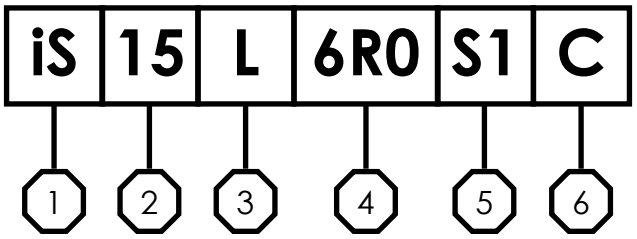
(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 1mA	150	-	-	V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 120V, T_J = 25°C	-	0.1	1	µA
		V_{GS} = 0V, V_{DS} = 120V, T_J = 125°C (2)	-	-	100	
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V	-	1	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 127µA	1.3	1.8	2.3	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 10V, I_D = 24A	-	5.1	6.0	mΩ
		V_{GS} = 4.5V, I_D = 12A	-	6.2	8.1	mΩ
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 24A	41	82	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance (2)	V_{GS} = 0V, V_{DS} = 75V, f = 100kHz	-	2,949	3,893	pF
C_{rss}	Reverse transfer capacitance (2)		-	37	64	
C_{oss}	Output capacitance (2)		-	144	187	
$C_{o(er)}$	Effective output capacitance	V_{DS} = 0 to 75V, V_{GS} = 0V	-	356	-	
R_G	Series gate resistance	f = 1MHz	-	1.1	1.5	Ω
$t_{d(on)}$	Turn-on delay time	V_{DS} = 75V, V_{GS} = 10V, I_{DS} = 24A, $R_{G,EXT}$ = 0 Ω	-	TBD	-	ns
t_r	Rise time		-	TBD	-	
$t_{d(off)}$	Turn-off delay time		-	TBD	-	
t_f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q_g	Gate charge total (2)	V_{DS} = 75V, I_D = 24A, V_{GS} = 0 to 10V	-	48	63	nC
Q_{sw}	Switching charge (3)		-	4.9	-	
Q_{gd}	Gate to drain charge (2)		-	3	4.2	
$Q_{g(th)}$	Gate charge at threshold (3)		-	5.8	-	
Q_{gs2}	Gate to source charge (3)		-	1.9	-	
$V_{plateau}$	Gate plateau voltage		-	3.7	-	V
Q_{oss}	Output charge (2)	V_{DS} = 0 to 75V, V_{GS} = 0V	-	132	170	nC
E_{oss}	Capacitive stored energy		-	1	-	µJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 24A, V_{GS} = 0V	-	0.8	0.9	V
Q_{rr}	Reverse recovery charge	V_{DS} = 75V, I_F = 24A, di/dt = 100A/µs	-	68	-	nC
t_{rr}	Reverse recovery time		-	68	-	ns

(2) Defined by design. Not subject to production test.
(3) Q_{SW} should be used for switching loss calculations. For more information see Qsw application note on www.idealsemi.com

DEVICE DECODER RING

Device Code



1 – iDEAL Semiconductor product

2 – Voltage rating divided by 10 (150V)

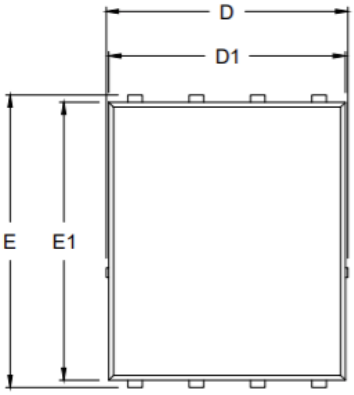
3 – L = N-Channel MOSFET, Logic Level Threshold

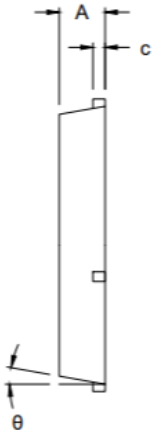
4 – Maximum drain-to-source resistance

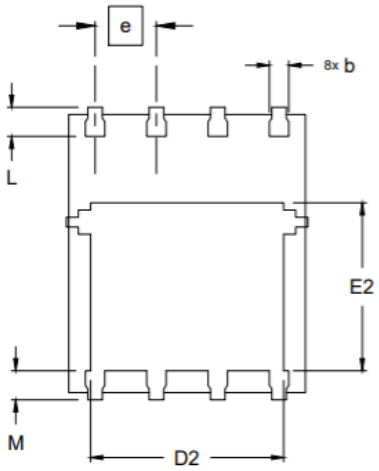
5 – SuperQ™ Generation

6 – C = PDFN 5x6mm

PDFN 5x6mm







SYMBOL	MIN	MAX
A	0.95	1.05
b	0.31	0.51
c	0.25 REF	
D	4.94	5.30
D1	4.80	5.1
D2	3.70	4.10
E	5.97	6.35
E1	5.67	6.10
E2	3.37	3.76
e	1.27 TYP	
L	0.51	0.71
M	0.51	0.73
θ	0°	10°

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Mailing Address:

iDEAL Semiconductor Devices, Inc.
116 Research Drive
Bethlehem, Pennsylvania, USA 18015
info@idealsemi.com