

SuperQ® 150V N-Channel Power MOSFET

5.5mΩ, 134A, PDFN 5X6

FEATURES

- Low on-resistance, $R_{DS(on)}$
- N-channel, logic level threshold
- Ultra low energy stored, E_{OSS}
- 100% UIS tested in production

APPLICATIONS

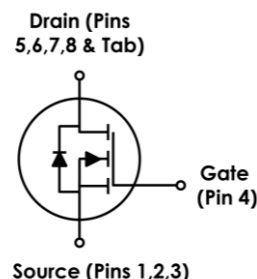
- Synchronous rectification with 5V gate drive
- SMPS control FETs

PRODUCT SUMMARY

Parameter	Typ	Max	Unit
V_{DS}		150	V
$R_{DS(on)}$ @ 10V	5.0	5.5	mΩ
I_D		134	A
Q_G	53	69	nC
Q_{SW}	5.4		nC
E_{OSS}	1.1		μJ

DESCRIPTION

This 150V SuperQ power MOSFET, with a typical $R_{DS(on)}$ of 5.0mΩ_{TYP}, is designed for synchronous rectification using 5V gate drive. Optimized for low Q_{RR} , Q_G , and E_{OSS} , the device reduces reverse recovery and switching losses, supporting high frequency operation and improved efficiency in DC-DC conversion stages.



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 16	V
I_D	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	134	A
	Continuous drain current (silicon limited), $T_C = 100^\circ\text{C}$	85	
I_{DM}	Pulsed drain current	434	
I_S	Continuous diode forward current, $T_C = 25^\circ\text{C}$	134	
$I_{S, PULSE}$	Diode pulse current	434	
P_D	Power dissipation, $T_C = 25^\circ\text{C}$	208	W
T_J, T_{SG}	Operating junction, storage temperature	-55 to 150	°C
E_{AS}	Avalanche energy, single pulse $I_D = 11.3\text{A}$, $R_{GS} = 25\Omega$	641	mJ

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
$R_{\theta JC}$	Junction-to-case thermal resistance – PDFN 5X6	-	-	0.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	°C/W

(1) 40mm x 40mm x 1.5mm epoxy PCB FR4 with a 6 cm² (one-layer, 70μm thick) copper area for drain connection. PCB is vertical in still air.

ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS15L5R5S1C	PDFN 5X6	iS15L5R5S1	13" 5,000pcs T&R

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

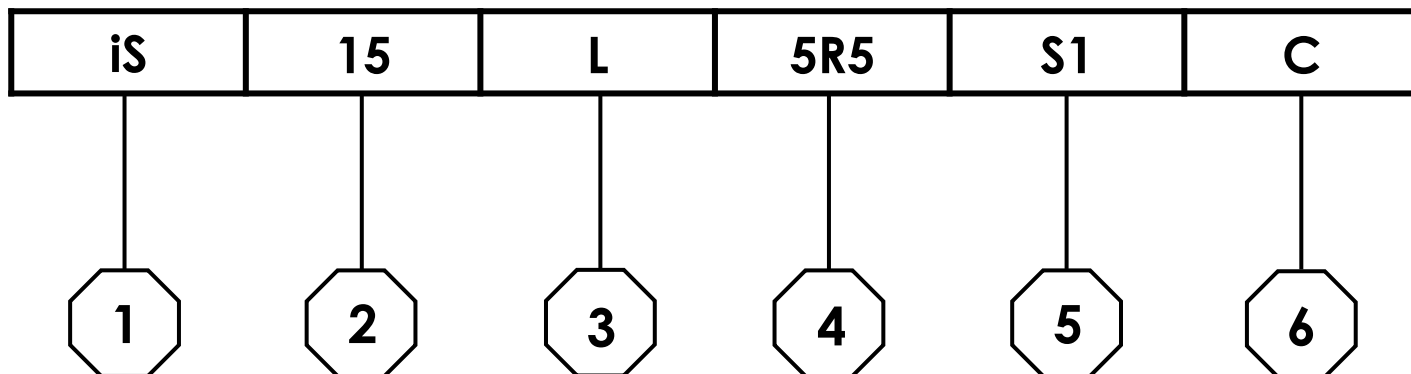
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	150	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 120V, T _J = 25°C	-	0.1	1.0	μA
		V _{GS} = 0V, V _{DS} = 120V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	1.0	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 140μA	1.3	1.8	2.3	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 25A	-	5.0	5.5	mΩ
		V _{GS} = 4.5V, I _D = 13A	-	6.1	8.0	
g _{fs}	Transconductance	V _{DS} = 10V, I _D = 25A	45	90	-	S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 75V, f = 100kHz	-	3,245	4,218	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	41	53	
C _{oss}	Output capacitance ⁽²⁾		-	158	206	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 75V, V _{GS} = 0V	-	373	-	
R _g	Series gate resistance	f = 1MHz	-	1.0	1.5	Ω
T _{d(on)}	Turn-on delay time	V _{DS} = 75V, V _{GS} = 10V, I _{DS} = 25A, R _{G,EXT} = 0Ω	-	TBD	-	ns
T _r	Rise time		-	TBD	-	
T _{d(off)}	Turn-off delay time		-	TBD	-	
T _f	Fall time		-	TBD	-	
GATE CHARGE CHARACTERISTICS						
Q _g	Gate charge total ⁽²⁾	V _{DS} = 75V, I _D = 25A, V _{GS} = 0 to 10V	-	53	69	nC
Q _{sw}	Switching charge ⁽³⁾		-	5.4	-	
Q _{gd}	Gate to drain charge ⁽²⁾⁽³⁾		-	3.3	4.3	
Q _{g(th)}	Gate charge at threshold ⁽³⁾		-	6.4	-	
Q _{gs2}	Gate to source charge ⁽³⁾		-	2.1	-	
V _{plateau}	Gate plateau voltage		-	3.7	-	V
Q _{oss}	Output charge ⁽²⁾	V _{DS} = 0 to 75V, V _{GS} = 0V	-	145	189	nC
E _{oss}	Capacitive stored energy		-	1.1	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 25A, V _{GS} = 0V	-	0.8	0.9	V
Q _{RR}	Reverse recovery charge	V _{DS} = 75V, I _F = 25A,	-	68	-	nC
t _{rr}	Reverse recovery time	di/dt = 100A/μs	-	68	-	ns

(2) Defined by design. Not subject to production test

(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for definitions of gate charge. For more information, see Q_{sw} application note on www.idealsemi.com

DEVICE DECODER RING

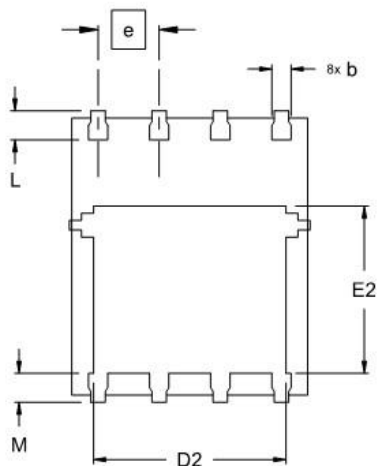
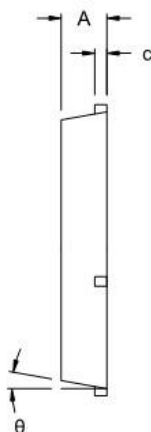
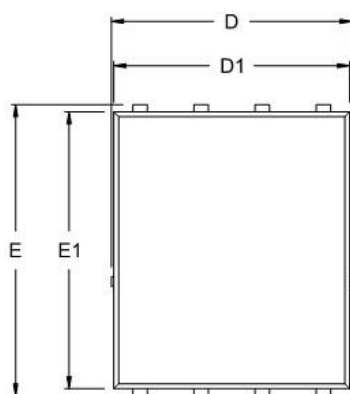
DEVICE CODE:



	— iDEAL Semiconductor product
	— Voltage rating divided by 10 (150V)
	— L = N-Channel MOSFET, Logic Level Threshold
	— Maximum drain-to-source resistance
	— SuperQ Generation
	— C = PDFN 5X6mm

Package Drawing

PDFN 5X6mm Package



SYMBOL	MIN	MAX
A	0.95	1.05
b	0.31	0.51
c	0.25 REF	
D	4.94	5.30
D1	4.80	5.1
D2	3.70	4.10
E	5.97	6.35
E1	5.67	6.10
E2	3.37	3.76
e	1.27 TYP	
L	0.51	0.71
M	0.51	0.73
θ	0°	10°

Revision History

Revision History		
Version	Date	Comments
Preliminary 1.0	September 2026	Preliminary Release

Scan or click QR code
for more information and
design resources:



IMPORTANT NOTICE AND DISCLAIMER

IDEAL SEMICONDUCTOR DEVICES, INC. ("IDEAL") PROVIDES THE DATASHEET AND ALL SUPPORTING DESIGN RESOURCES, SAFETY INFORMATION, AND OTHER MATERIALS (THE "RESOURCES") "AS IS". IDEAL AND/OR ITS LICENSORS DO NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE RESOURCES OR THAT SUCH RESOURCES WILL BE SUITABLE FOR YOUR APPLICATION. IDEAL HEREBY DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, OR NON-INFRINGEMENT.

You are only permitted to use the Resources and any products provided by iDEAL ("Products") in accordance with the operating parameters set forth in the Resources and iDEAL's standard terms and conditions made available at the time of order placement. Please note that the Resources are intended for skilled, technically trained developers. You are solely responsible for, and iDEAL disclaims all responsibility and liability for: (a) choosing the Products and evaluating the suitability of such Products for the intended application, as well as determining if the information in the Resources is complete for your application; (b) designing, validating and testing the Products in your system; and (c) ensuring your application meets applicable safety, security, regulatory or other industry requirements and standards. iDEAL assumes no liability for any damage or malfunction resulting from improper handling of Products, or use of Products and Resources outside of the specified parameters. You are responsible for consulting the latest datasheet before placing orders.

iDEAL reserves the right to make corrections, modifications, enhancements, improvements, and other changes to or otherwise discontinue its Resources and Products in its sole discretion at any time without notice. All Products are sold subject to iDEAL's standard terms and conditions made available at the time of order placement.

PRODUCT STATUS

PRELIMINARY DATASHEET and PRODUCT PREVIEW concern products in the formative or design phase of development. Characteristic data and other specifications are measured and also design goals. iDEAL Semiconductor Devices, Inc. ("iDEAL") reserves the right to change or discontinue these products without notice.

SuperQ® is a registered trademark of iDEAL Semiconductor Devices, Inc.

Mailing Address:

IDEAL Semiconductor Devices, Inc.
116 Research Drive
Bethlehem, Pennsylvania, USA 18015
info@idealsemi.com